AN12330

TEA2016 PFC + LLC controller IC

Rev. 1 — 28 November 2019 Application note

Document information

Information	Content
Keywords	TEA2016AAT, PFC, LLC, burst mode operation, low-power mode, resonant power converter, programmable settings.
Abstract	The TEA2016AAT is a controller IC for resonant power supplies that include a PFC. It provides high efficiency at all power levels. Together with the TEA1995T dual LLC resonant SR controller, a high performance cost-effective resonant power supply can be made. To reach a high efficiency at all power levels, the TEA2016AAT provides a low-power operation mode (LP) and extensive burst mode configuration options. Most LLC resonant converter controllers regulate the output power by adjusting the operating frequency. The TEA2016 regulates the output power by adjusting the voltage across the primary resonant capacitor for accurate state control and a linear power control. Parameter settings in an internal multitimes programmable memory can define operation modes and protections. For product development, an IC version is available to make setting changes on the fly. This feature provides flexibility and ease of design to optimize controller properties to application-specific application requirements. The TEA2016AAT provides extra functions like active X-capacitor discharge, external OTP sensing, and power good signal. Protections can be configured to provide the correct handling for overcurrent protection (OCP), overvoltage protection (OVP), overpower protection (OPP), power limitation, brownin, brownout, capacitive mode regulation (CMR), undervoltage protection (UVP), overtemperature protection (OTP), and open-loop protection (OLP).

Revision history		
Rev	**Date**	**Description**
v.1	20191128	initial edition

1 Introduction

The TEA2016AAT is a fully digital controller for high-efficiency PFC and resonant power supplies. Together with the TEA1995T dual SR controller, a complete resonant power supply can be built which is easy to design and has a very low component count. This power supply meets the efficiency regulations of Energy Star, the Department of Energy (DoE), the Eco-design directive of the European Union, the European Code of Conduct, and other guidelines. An auxiliary low-power (standby) supply can be omitted.

This application note discusses the TEA2016AAT functions for different applications in general. Because the IC with two controllers provides extensive functionality, many subjects are discussed.

This document is set up in such a way, that a chapter or paragraph of a selected topic can be read as a standalone explanation with a minimum number of cross-references to other document parts or the TEA2016AAT data sheet. The consequence is repetition of some information within the application note and descriptions or figures that are similar to the ones published in the data sheet. In most cases, to enhance the readability, only typical values are given.

1.1 Related documents

Additional information and tools can be found in other TEA2016 documents such as:

- TEA2016AAT data sheets
- Excel calculation sheet (available on request)
- Demo board user manuals
- USB-I^2C interface user manual
- Ringo graphical user interface software user manual

1.2 Related products

NXP Semiconductors products related to the TEA2016AAT are:

- TEA1716:
  This product provides a PFC+LLC controller in a SO24 IC package and allows low power consumption burst mode operation.
- TEA1916
  This product provides a PFC+LLC controller combo with two ICs in a SO8 (PFC TEA19162) and SO16 (LLC TEA19161) package is suitable for applications that have high requirements on burst mode operation. It offers extra functions and several operation settings for flexible power supply design.

Other NXP Semiconductors products for resonant power conversion are:

- TEA1795:
  Synchronous rectification controller for resonant converters with dual gate drivers in SO8
- TEA1995T:
  Synchronous rectification controller for resonant converters with dual gate drivers in SO8. This product is optimized for the TEA2016 operating modes.
- TEA1708:
  X-capacitor discharge IC
- TEA2095T/TEA2095TE
  Synchronous rectification controller for resonant converters with dual gate drivers in SO8. It is similar to the TEA1995T. It can drive MOSFETs with a lower R_{DSon} and has an output discharge function.

2 TEA2016AAT highlights and features

2.1 Resonant conversion

Today, the market demands high-quality, reliable, small, lightweight, and efficient power supplies.

A resonant DC-to-DC converter produces sinusoidal currents with low switching losses. It provides the possibility of operation at higher frequencies with excellent efficiency at high power levels.

In the recent years, LLC resonant converters have become very popular because of the high efficiency at medium and high output load they offer. It is the generation of resonant controllers that supports burst mode operation has also enabled good efficiency at low output load and a low power consumption in standby or no-load operation.

The TEA2016AAT offers a next step in design flexibility and production optimization. It offers the programming of many settings in an internal multiple times programmable (MTP) memory. During the design phase, settings can be modified on the fly to obtain the best performance for each application.

2.2 Power factor correction conversion

Basic switch-mode power supplies represent a non-linear impedance (load characteristic) to the mains input. The current taken from the mains supply occurs only at the highest voltage peaks and is stored in a large capacitor. The energy is taken from this capacitor, in accordance with the switch mode power supply operation characteristics.

Government regulations dictate special requirements for the load characteristics of certain applications.

Two main requirements:

- Mains harmonics requirements EN61000-3-2
- Power factor (real power/apparent power)

The requirements impose a more resistive characteristic of the mains load.

To fulfill these requirements, measures must be taken regarding the input circuit of the power supply. Passive (typically a series coil) or active (typically a boost converter) circuits can be used to modify the mains load characteristics accordingly.

An additional market requirement for the added mains input circuit is that it works with a good efficiency and at low cost.

Using a boost converter to meet these requirements, provides the benefit of a fixed DC input voltage for a resonant converter. The fixed input voltage allows an easier design of the resonant converter (especially for wide mains input voltage range applications) and the possibility to achieve a higher efficiency.

2.3 TEA2016AAT digital PFC+LLC controller

The TEA2016AAT provides high efficiency at all power levels. Together with the TEA1995T, dual LLC resonant SR controller, a high-performance cost-effective resonant power supply can be made. A power supply that meets the efficiency regulations of Energy Star, the Department of Energy (DoE), the Eco-design Directive of the European Union, the European Code of Conduct, and other guidelines.

In general, resonant converters show an excellent efficiency at high power levels, while at lower levels their efficiency reduces because of the relatively high magnetizing current losses. To reach a high efficiency at all power levels, the TEA2016AAT provides a low-power operation mode (LP) and extensive burst mode configuration options.

Most LLC resonant converter controllers regulate the output power by adjusting the operating frequency. The TEA2016AAT regulates the output power by adjusting the voltage across the primary resonant capacitor for accurate state control and a linear power control.

The primary resonant capacitor voltage provides accurate information about the output power to the controller by a voltage divider. The voltage divider sets the output power levels. It determines when the system switches from the high-power mode to low-power mode and when it switches from low-power mode to burst mode.

To define operation modes and protections, many parameter settings are available. These parameters can be stored/programmed in an internal memory. The feature provides flexibility and ease of design to optimize controller properties to application-specific requirements or even optimize/correct performance during power supply production. At start-up, the IC loads the parameter values for operation. For easy design work during product development, an IC version is available to change settings on the fly.

2.4 Features and benefits

2.4.1 Distinctive features

- Universal mains supply operation (70 V (AC) to 276 V (AC))
- Integrated high-voltage start-up
- Integrated X-capacitor discharge
- Second PFC output OVP
- SUPIC regulation by HV source allowing small SUPIC capacitor
- Fast system start-up (< 0.5 s)
- Integrated high-voltage level shifter
- LLC and PFC burst mode soft start/stop for audible noise reduction
- LLC and PFC soft start at startup
- Power Good signal
- External OTP NTC sensing
- Up to 500 kHz half-bridge switching frequency
- Ease of design by programmable operation and protection parameters

2.4.2 Green features

- PFC valley/zero voltage switching for minimum switching losses
- PFC frequency limitation for best efficiency by reduced switching losses
- Very high system efficiency at all load conditions
- Compliant with Energy using Product directive (EuP) lot 6
- Excellent no-load system input power (< 75 mW)
- Regulated low feedback optocoupler current, enabling low no-load power consumption
- Very low IC supply current during non-switching state in burst mode
- LLC adaptive non-overlap time

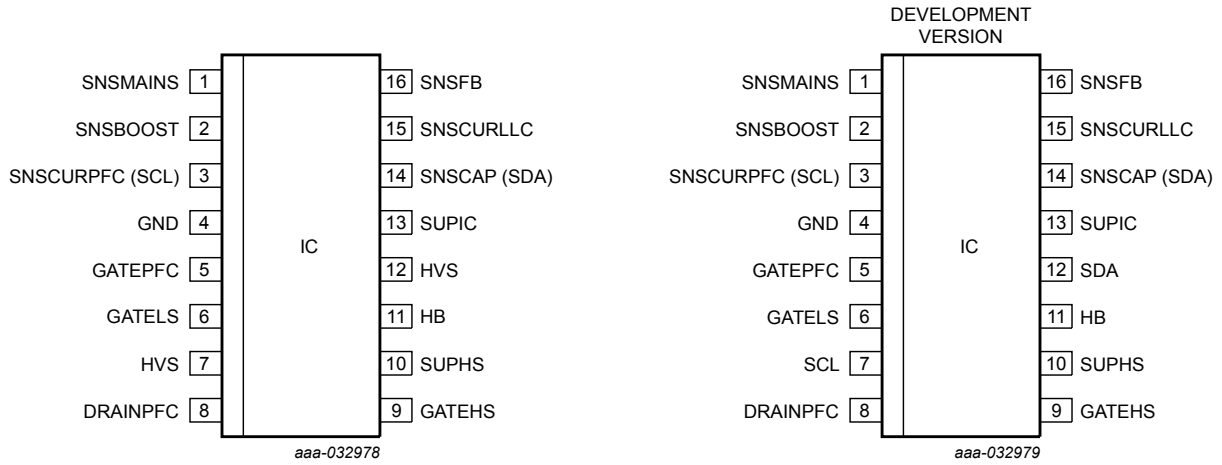
2.4.3 Protection features

- Safe restart, latched, or latched-after-safe-restart option for system fault conditions
- PFC continuous mode protection with demagnetization detection
- Accurate PFC output overvoltage protection (OVP)
- Open control loop protection
- Internal and external IC overtemperature protection (OTP)
- Low and adjustable PFC overcurrent protection (OCP) trip level
- Adjustable brownin/brownout protection
- Supply undervoltage protection (UVP)
- Two overpower protection (OPP) levels and power limiting
- Programmable overpower timeout
- Capacitive mode protection (CMR)
- Maximum LLC on-time protection for low-side and high-side
- Overcurrent protection (OCP)
- Disable input

2.5 Typical areas of application

- High-power adapters (TV, gaming console,…)
- Slim notebook adapters
- Computer desktop or all-in-one power supplies
- LCD television or computer monitor
- Office equipment
- Server supplies
- High-power IOT supplies

3 TEA2016AAT pin overview with functional description summary



a. Normal version

b. Development version

Figure 1. TEA2016AAT pinning diagrams

Table 1. Pin overview

Pin	Name	Functional description summary
1	SNSMAINS	This pin combines two functions. The functions are alternately active in time. **Mains voltage sensing** During the mains voltage sensing, the SNSMAINS pin voltage is high enough to disable interference from the OTP network. For mains sensing, the current flowing in the SNSMAINS pin is measured. The current depends on the external resistor value. A choice can be made to use 10 MΩ or 20 MΩ and to 1 resistor to 1 mains connection or 2 resistors to both mains connections. During a half-mains voltage cycle, the peak current value is determined and stored. The value is used as an input for • Mains compensation function of the PFC regulation loop • Brownin and brownout function At a selectable current level of 4.95 µA to 13.35 µA, the brownin level is reached and the IC starts switching. When the current drops again under the selectable hysteresis relative to the brownin level 0.15 µA to 1.2 µA, the brownout level is reached and the IC switching stops. When after brownout the brownin level is reached again, a latched protection state is reset. If during a selectable delay of 100 ms to 400 ms mains is detected, the X-capacitor discharge function is activated. During the X-capacitor discharge mode, the SNSMAINS current is monitored for reconnecting the mains again. The X-capacitor discharge function can be disabled by selecting the infinite delay option. **External NTC overtemperature protection (OTP)** The OTP measurement is done at the top of the mains voltage, just after the mains measurement has finished the peak detection. During 50 µs, a selectable (150 µA to 1050 µA) current flows from the pin through the external diode and NTC to ground. The resulting voltage on pin is measured. When the voltage on the pin is below 3 V during a selectable time (0.5 s to 8 s), the OTP protection is activated.
2	SNSBOOST	This pin combines four functions. The boost voltage is sensed for: • Sensing the boost voltage for PFC output voltage regulation • Brownin and brownout of the LLC • LLC input voltage compensation: adapting the V_{cap} levels to keep a constant output power level at varying input voltage. • System enable and disable: Pulling SNSBOOST to GND disables the system and hold or stop operation.

Pin	Name	Functional description summary
3	SNSCURPFC	**Current sense input for PFC or I^2C-SCL** A sense resistor that measures the converter current provides a (mainly) negative voltage on SNSCURPF. A series resistor prevents excessive voltage on the IC pin during start-up and surge events. **PFC OCP** This input is used to limit the maximum peak current in the PFC coil. The current sense input provides a cycle-by-cycle protection. When the SNSCURPFC level reaches −300 mV, the PFC MOSFET is switched off. The external sense resistor value determines the current value. **PFC demagnetization** The signal is used to detect demagnetization when the voltage rises above −10 mV.
4	GND	**Ground** Reference for driver and measurement inputs.
5	GATEPFC	**Gate driver output for PFC MOSFET**
6	GATELS	**Gate driver output for low-side MOSFET of LLC** A resistor measurement function in the IC measures the value of the resistor to GND. Applying a certain resistor value gives the option to select one of the 4 preselected “menus”. Each "menu" consisting of a group of basic settings related to protections. It mainly offers a choice between safe restart or latched follow-up character.
7	HVS or SCL	• **Normal IC version:** Not connected, high-voltage spacer. • **Development IC version:** SCL clock I/O for I^2C communication

Pin	Name	Functional description summary
8	DRAINPFC	This pin combines four functions • High-voltage supply input for the HV start-up source to charge SUPIC • Drain voltage valley detection for PFC operation • Second PFC output OVP sensing • Active X-capacitor discharge **HV source** The HV source charges SUPIC to the start level of 19 V and regulates it with a hysteresis of 0.7 V. During the non-switching period in burst mode, the HV source is activated when the SUPIC voltage drops to 12 V. To avoid the system from stopping during a very long period of non-switching, the HV source regulates the SUPIC voltage with a hysteresis of 0.7 V above 10 V. **Valley detection** To minimize switching losses, the valley of the drain voltage ringing is detected for switching on the PFC MOSFET at the lowest voltage level after demagnetization. **Second PFC output OVP** The maximum voltage is detected for sensing the PFC output voltage. If the main PFC output OVP function on SNSBOOST fails, the sensing on DRAINPFC provides a backup protection. The levels for the DRAINPFC OVP function are higher and less accurate. **Active X-capacitor discharge** The HV source can be switched to GND instead of to SUPIC internally. It provides a discharge function for the mains input circuit including the X-capacitors. When mains disconnection is detected at SNSMAINS, this source is activated after a selectable time delay.
9	GATEHS	**Gate driver output for high-side MOSFET of LLC**
10	SUPHS	**High-side driver supply** Connected to an external bootstrap capacitor between HB and SUPHS. The supply is obtained by using an external diode between GATELS and SUPHS.
11	HB	**Reference for the high-side driver GATEHS** HB is externally connected to a half-bridge node between the MOSFETs of LLC. It is an input for the internal half-bridge slope dV/dt detection circuit for adaptive non-overlap regulation and top-switching in LP mode.
12	HVS or SDA	• **Normal IC version:** Not connected, high-voltage spacer. • **Development IC version:** SDA data I/O for I2C communication

Pin	Name	Functional description summary
13	SUPIC	**IC voltage supply input and output of the HV start-up source.** All internal circuits are supplied from this pin, except for the high-voltage circuit. The buffer capacitor on SUPIC can be charged or supplied in several ways: • High-voltage (HV) start-up source • Auxiliary winding from LLC transformer or capacitive supply from switching half-bridge node • External DC supply, for example a standby supply When the SUPIC voltage has reached the start level of 19 V or 12 V (selectable), the IC enables operation. If supplied by the HV source, the voltage is regulated with a hysteresis of 0.7 V. The IC stops operation below 10 V. A system reset is activated at 9 V. During the non-switching period in burst mode, the HV source is activated when the SUPIC voltage drops to 12 V. To avoid the system from stopping during a very long period of non-switching, the HC source regulates the SUPIC voltage with a hysteresis of 0.7 V above 10 V. For protection purposes, the SUPIC voltage is also sensed for a selectable overvoltage level. When an auxiliary winding from the LLC transformer is used, the SUPIC voltage reflects the converter output voltage.
14	SNSCAP	**Senses the voltage on the LLC capacitor for driving the correct output power or I^2C-SDA.** SNSCAP is externally connected to a resistive + capacitive divider to the voltage on the resonant capacitor. An internal bias circuit generates a 2.5 V (DC) level on SNSCAP. The divider scales the voltage levels on the resonant capacitor for the power level control range from 0 % to 200 % power to the maximum SNSCAP range of 1 V to 4 V, including input voltage compensation. The scaling sets the correct levels for • transition level HP/LP and LP/BM • minimum energy per cycle (ECmin at LP/BM transition) • OPP level • 200 % power level and power limit For each half cycle, the internal power control sets a new target SNSCAP voltage level for switching off the LLC MOSFET for the required power. It is based on • SNSFB current (feedback regulation) • SNSBOOST voltage (input voltage compensation) • Mode transition control • Slope compensation (power reduction during startup and protection) • HB symmetry regulation (variable bias current source)

Pin	Name	Functional description summary
15	SNSCURLLC	**Sense input for the momentary primary current of the LLC** By a voltage across and external measurement resistor. A series capacitor applies the voltage signal to the pin. To avoid disturbance, the capacitor must be very close to the pin. The IC biases the DC voltage on the pin to 2.5 V. Internal voltage levels are: • If SNSCURLLC − V_{BIAS} exceeds ±1.5 V, the gate driver is switched off to limit the power to the OCP level. After a selectable number of OCP cycles, the protection is activated. • SNSCURLLC − V_{BIAS} ± a selectable low-voltage level for detecting the (almost) zero current level. To prevent capacitive mode switching, the driver switches off at this level. • SNSCURLLC − V_{BIAS} ± 13 mV for detecting the current polarity. It is used as parameter in the internal switching logic.
16	SNSFB	**Sense input for LLC output regulation feedback by current and power good signal** Normally, the pin is connected via an optocoupler to ground. Pulling current from SNSFB regulates the power. The IC measures the regulation current. An additional 100 Ω series resistor to GND can be useful for measuring the current during engineering work. To minimize power consumption, the internal source slowly regulates the SNSFB to an average low current level. It is called the optobias regulation. The bias value can be selected by setting between 80 µA and 1200 µA. The value for BM operation is 20 % higher. The SNSFB current and voltage level are now independent from the output power. Changes in the required power level regulated by SNSFB current variations. **Power good** The SNSFB pin can be pulled to a high voltage level to provide a power good (PG) signal. This signal shows the status of stable operation after start-up and provides a warning that the supply is soon shut down.

4 Application diagram

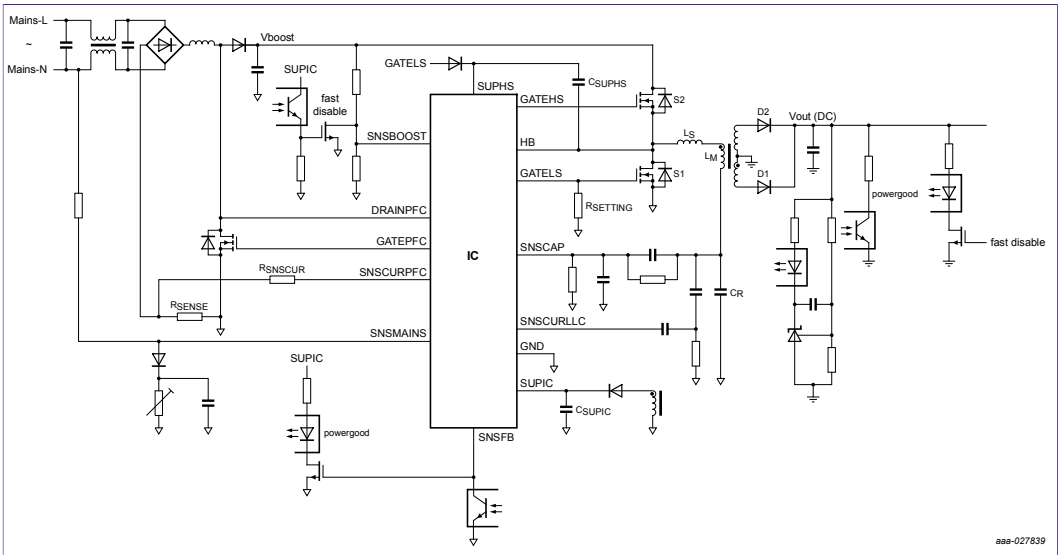


Figure 2. Basic application diagram TEA2016AAT

5 Block diagram

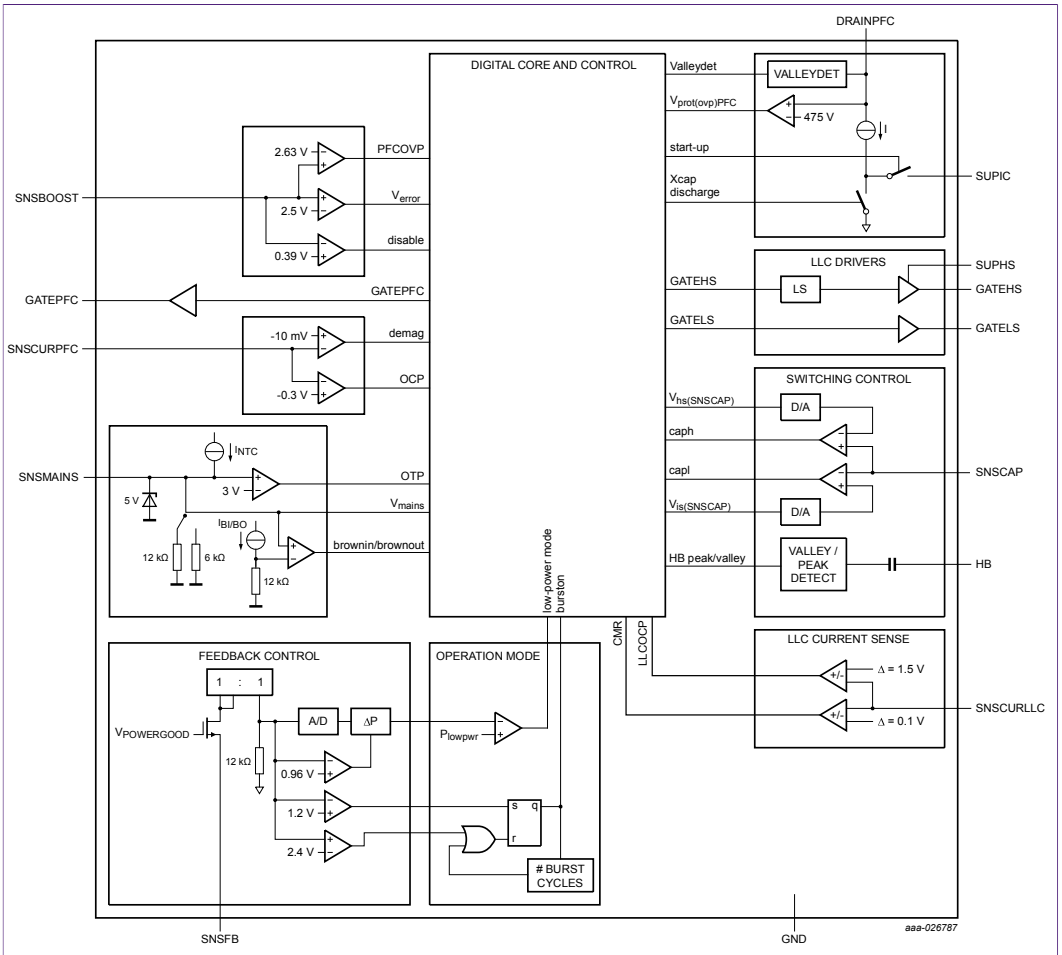


Figure 3. Block diagram TEA2016AAT PFC + LLC controller

6 Supply functions and start-up

6.1 Basic supply system overview

The TEA2016AAT has a high-voltage supply pin for start-up (DRAINPFC) and a general supply (SUPIC).

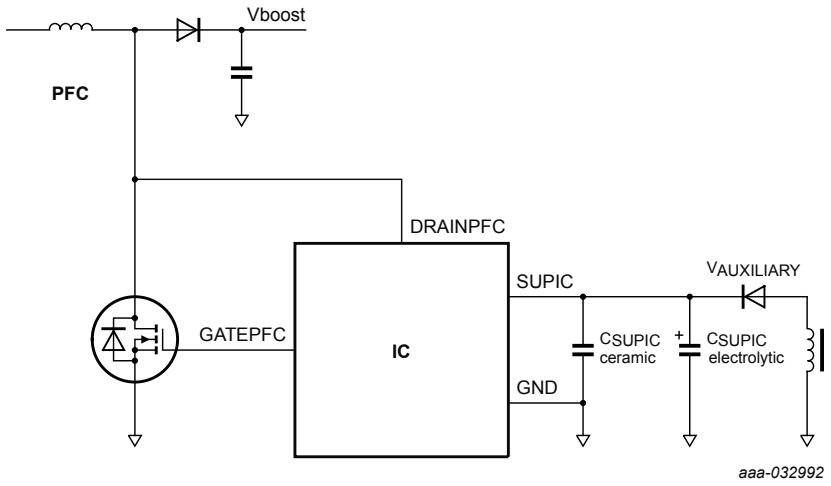


Figure 4. TEA2016AAT basic IC supply application

6.2 DRAINPFC high-voltage supply

The TEA2016AAT uses an internal current source connected to DRAINPFC to start up. This current source also provides the IC supply in a latched protection state or in the off state. To prevent that the SUPIC undervoltage protection is triggered, the source is also activated when the SUPIC voltage becomes too low.

6.2.1 Start-up (DRAINPFC)

Initially, the DRAINPFC source charges the capacitors on the SUPIC pin.

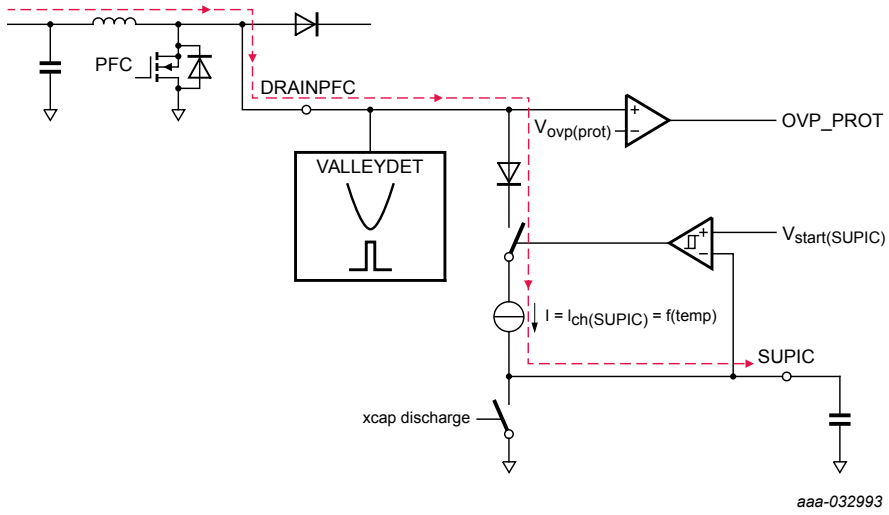


Figure 5. TEA2016AAT DRAINPFC functions and SUPIC charging path

The internal current source function delivers 8.5 mA. If a fault condition occurs, the charge current is reduced when the internal IC temperature of the source circuit reaches its maximum value.

When the SUPIC reaches the start level of typically 19 V, when opening/closing the internal source switch, the voltage is regulated with a 700 mV hysteresis.

Several other tasks are done during start-up:

- Copying the MTP settings in the registers
- Checking that the signal levels are correct before start-up is enabled. Like bias voltage on SNSCURLLC and SNSCAP, SNSBOOST > 2.3 V and other protection levels

6.2.2 Start-up - protection - restart - stop sequence

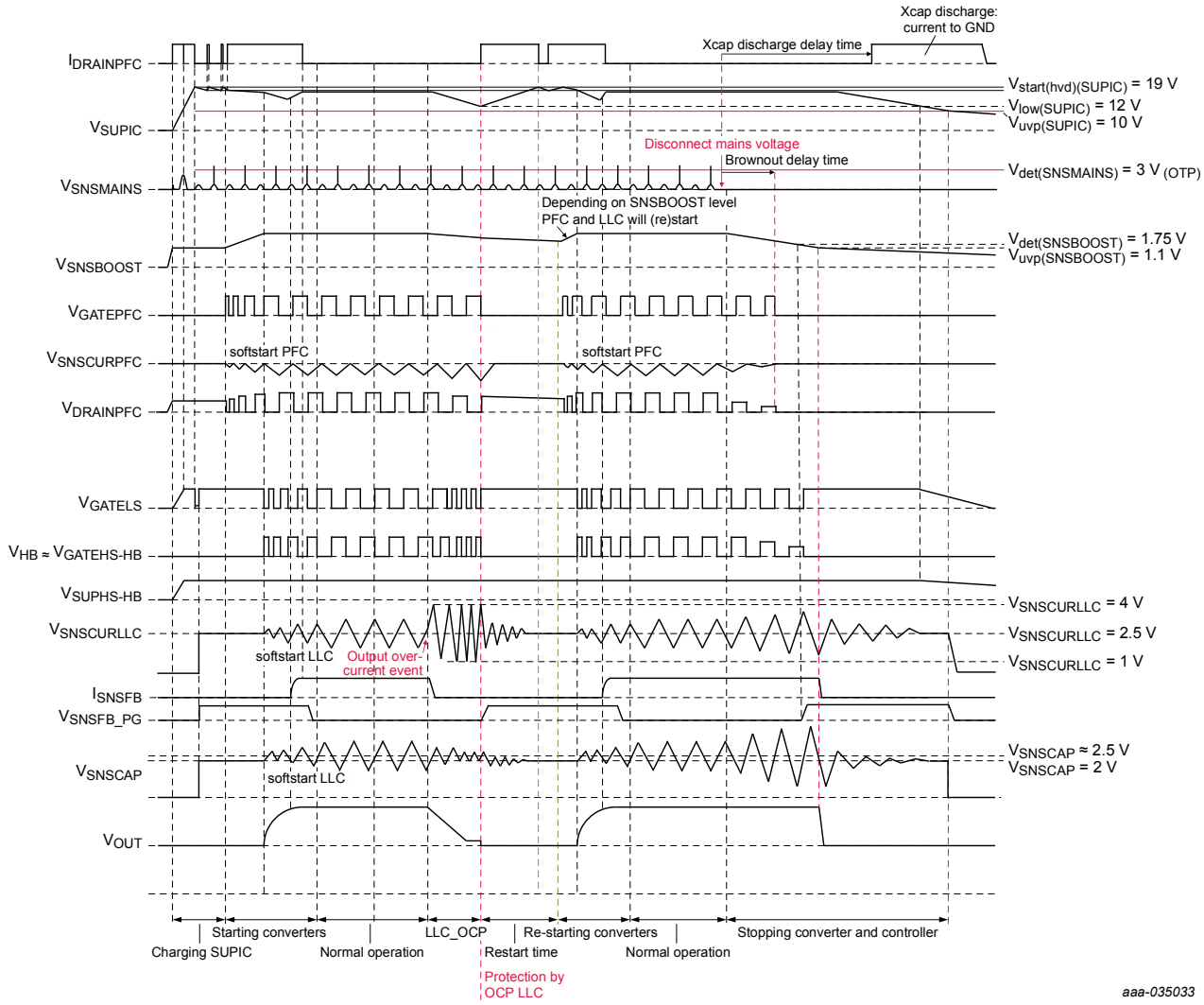


Figure 6. TEA2016AAT signal sequences: start-up – protection - restarting - stopping

6.2.3 DRAINPFC during burst mode operation

When the SUPIC voltage temporarily drops to a low value during burst mode, the DRAINPFC source can be activated. It can happen, for example, when there is a long period of non-switching after a load step. In this situation, the supply from the auxiliary winding does not generate energy for a long time while the IC still consumes a low amount of current.

During the non-switching period of the burst mode, the HV source is activated when the SUPIC voltage drops below 11 V. The DRAINPFC source regulates the SUPIC voltage with a hysteresis of 700 mV. This emergency function prevents that the system stops and restarts when an accidental condition occurs, because it triggers the SUPIC UVP level on 10 V.

6.3 SUPIC supply using LLC transformer auxiliary winding

An auxiliary winding on the LLC transformer can be used to obtain a supply voltage for the SUPIC pin during operation. As the SUPIC pin has a wide operational voltage range (10 V to 36 V), it is not a critical parameter.

However:

- The voltage on the SUPIC pin must be low to minimize power consumption.
- During burst mode operation and because of the low current consumption of the supply, the bursts repetition frequency can become very low (for example at no output load). This behavior can cause an imbalance in the half-bridge switching leading to a serious drop in the auxiliary supply for the SUPIC pin. To maintain the LLC load balance and avoid the extra SUPIC pin voltage drop, replace a single-side rectified auxiliary supply with a center-tapped construction. The center-tapped construction comprises two windings and two diodes.
- To use the auxiliary winding voltage for the IC supply and LLC output voltage measurement (using SUPIC), the auxiliary winding supply must be an accurate representation of V_{OUT}. To ensure a good coupling, physically place the transformer auxiliary winding on the secondary output side. When the transformer contains separate sections for primary and secondary winding (see Figure 7), this aspect is more critical than on transformers that have all windings in one section.
- When mains insulation is included in the transformer, it can affect the auxiliary winding construction. When the transformer auxiliary winding is placed on the transformer construction secondary area, triple-insulated wire is required.

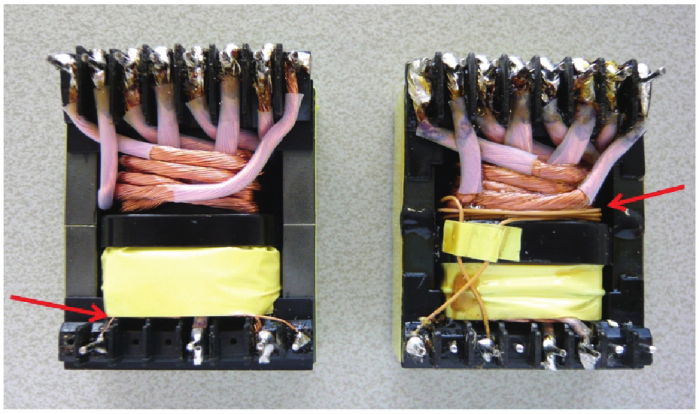


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Figure 7. Transformer auxiliary winding on primary side (left, not preferred) and secondary side (right)

Using the overvoltage function on SUPIC with a transformer auxiliary winding, a good representation of the output voltage measurement can only be obtained after addressing several issues.

An additional advantage of a good coupling/representation of the auxiliary winding with the output windings is that a stable auxiliary voltage is obtained for the SUPIC pin. A low SUPIC voltage value can be designed easier for the lowest power consumption.

6.3.1 Auxiliary supply voltage variations because of output current

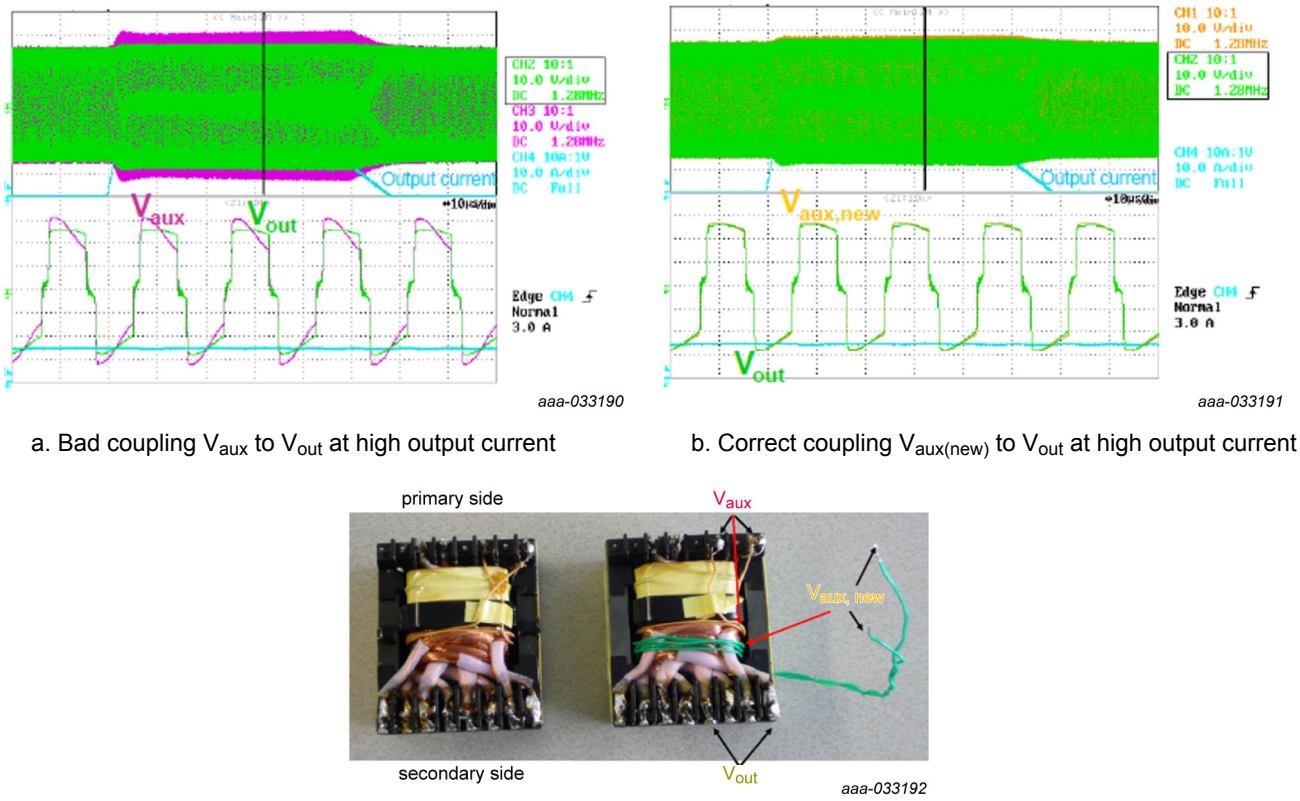
The LLC output causes variation on an auxiliary winding supply. At peak current loads, the regulation compensates the voltage drop across the series components in the LLC output stage (resistance and diodes). The result is a higher voltage on the windings at higher output currents because the higher currents cause a larger voltage drop across the series components.

In burst mode operation near no load, the number of pulses in time that charge SUPIC in time is limited. To prevent that the voltage drops severely. The rectifiers used in the auxiliary supply must be able to handle the high currents.

6.3.2 Voltage variations depending on auxiliary winding position: primary side component

The voltage on SUPIC can contain a number of unwanted primary voltage components due to a less optimal position of the auxiliary winding. When the transformer contains separate sections for primary and secondary winding (see type in Figure 7), this aspect is more critical than on transformers that have all windings in one section. This deviation can seriously endanger the feasibility of the SUPIC sensing function.

The coupling of the auxiliary winding with the primary winding must be as small as possible to avoid a primary voltage component on the auxiliary voltage. Place the auxiliary winding on the secondary windings and as physically remote as possible from the primary winding. The differences in results are shown in Figure 7 using comparison of the secondary side position.



a. Bad coupling V_{aux} to V_{out} at high output current

b. Correct coupling $V_{aux(new)}$ to V_{out} at high output current

c. Photograph

Figure 8. Example of a (new) position of the auxiliary winding for a better coupling to the output voltage

6.4 SUPIC pin supply using external voltage

When another (standby) power supply supplies TEA2016AAT SUPIC, the SUPIC start-up level can be set at a lower value: 12 V instead of 19 V.

6.5 SUPHS

An external bootstrap buffer capacitor supplies the high-side driver. The bootstrap capacitor is connected between the high-side reference the HB pin and the high-side driver supply input the SUPHS pin. When HB is low, an external diode from the GATELS pin charges this capacitor.

Selecting a suitable external diode can minimize the voltage drop between the GATELS and SUPHS pins. Minimizing the voltage drop is especially important when using a MOSFET that requires a large amount of gate charge and/or when switching at high frequencies.

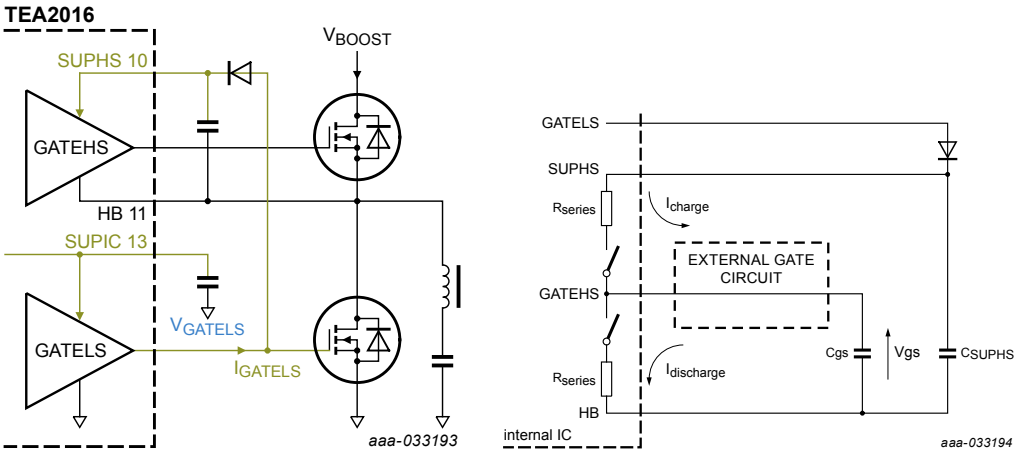


Figure 9. Supply system for GATEHS: GATELS charges SUPHS by bootstrap

6.5.1 Initial charging of the SUPHS pin

At start-up the GATELS switches the low side MOSFET on to charge C_{SUPHS} by the bootstrap function.

The current taken from the SUPHS pin consists of two parts:

- Internal MOSFET driver GATEHS
- Internal circuit to control the GATEHS pin

6.5.2 A lower voltage on SUPHS

During normal operation, each time the half-bridge node (HB) is switched to ground level, the bootstrap function charges C_{SUPHS}. The voltage value between the HB and SUPHS pins is normally lower than the voltage on the GATELS pin (or other bootstrap supply input) because of the voltage drop across the bootstrap diode.

The voltage drop across the bootstrap diode is directly related to the amount of current that is required to charge C_{SUPHS}. The resulting voltage between the SUPHS and HB pins depends also on the time available for charging.

A large voltage drop occurs when an external MOSFET with a large gate capacitance has to be switched at high frequency (high current + short time).

During burst mode operation, a (too) low voltage on the SUPHS pin can occur. In burst mode, there are (long) periods of not switching. Therefore, long periods of no charging of the SUPHS pin can occur. During this time, the circuit C_{SUPHS} slowly discharges the supply voltage capacitor. When a new burst starts, the SUPHS voltage is lower than during normal operation. During the first switching cycles, C_{SUPHS} is recharged to its normal level. At low output power during burst mode, the switching frequency is normally rather high. The high switching frequency limits fast recovery of the voltage between the SUPHS and HB pin.

Although in most applications the voltage drop is limited, it is an important issue for evaluation. The voltage drop can influence the selection of the best diode type for the bootstrap function and the value of the SUPHS pin buffer capacitor.

To prevent that switching becomes unreliable, the driver stops operation when the voltage across C_{SUPHS} drops to below 7 V.

6.6 Capacitor values on the SUPIC and SUPHS pins

An example of a practical application is provided in Section 17 (240 W power supply).

6.6.1 The SUPIC pin

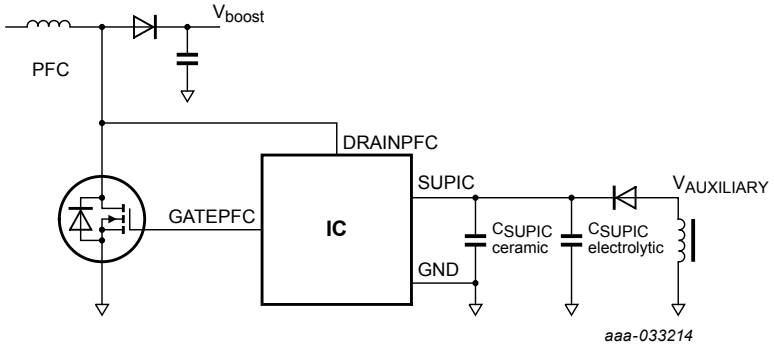


Figure 10. TEA2016AAT basic IC supply application

6.6.1.1 General

Use two types of capacitors on the SUPIC pin. An SMD ceramic type with a smaller value located close to the IC and an electrolytic type incorporating the major part of the capacitance.

Typical values are:

- $C_{SUPIC\_electrolytical}$ = 47 µF
- $C_{SUPIC\_ceramic}$ = 470 nF

6.6.1.2 Start-up

When an HV source provides the start-up energy, the SUPIC capacitor value can be small. However, it must be sufficient to handle the start-up during the period when the LLC starts until the auxiliary winding takes over the supply of the SUPIC pin.

Example of the basic value estimation:

- $I_{SUPIC(at\ start\ LLC)}$ = 25 mA
- $\Delta V_{SUPIC(startup)} = V_{start(SUPIC)} - V_{uvp(SUPIC)}$ = 19.0 V − 10 V = 9 V
- $\Delta t_{vaux\_>13V}$ = 10 ms
- $I_{DRAINPFC}$ = 7 mA (minimum value)

$C_{SUPIC} > (I_{SUPIC\_at\_startup} - I_{DRAINPFC}) \times (dt_{Vaux} / dV_{SUPIC(startup)}) =$
(25 mA − 7 mA) x (10 ms / 9 V) = 20 µF

6.6.1.3 Normal operation

The main purpose of the capacitors on SUPIC is to keep the current load variations (for example gate drive currents) local at normal operation.

6.6.1.4 Burst mode operation

When burst mode operation is applied, the supply construction often uses an auxiliary winding and start-up from the HV source. In the burst mode, there is a long period during which the auxiliary winding is not able to charge C_{SUPIC}. There is no LLC switching time between two bursts. To prevent that the DRAINPFC high-voltage source is activated (to keep SUPIC from dropping to the undervoltage protection level of 10 V), the capacitor value on SUPIC must be high enough to keep the voltage above 12 V. Activating the high-voltage source increases the power supply consumption considerably.

Example of the minimum C_{SUPIC} value estimation for burst mode:

- $I_{SUPIC\_between\_2\_bursts}$ = 0.7 mA
- $dV_{SUPIC\_in\_burst} = V_{auxilary\ in\_burst} - V_{SUPIC\_low}$ = 19 V – 12 V = 7 V
- $dt_{between\_2\_bursts}$ = 100 ms
- $C_{SUPIC} > I_{SUPIC\_between\_2\_bursts} \times (dt_{between\_2\_bursts} / dV_{SUPIC\_in\_burst})$ = 0.7 mA x (100 ms / 7 V) = 10 µF

6.6.2 Value of the capacitor for SUPHS

To support charging the gate of the high-side MOSFET, the SUPHS capacitor value must be much higher than the gate capacitance. It prevents that the voltage on SUPHS significantly drops by the gate charge.

To prevent that the SUPHS voltage becomes too low during a long the time between two bursts, the GATEHS driver circuit only uses a very small amount of current in the burst energy save state.

7 MOSFET drivers GATELS, GATEHS, and GATEPFC

The TEA2016AAT provides three outputs for driving external high-voltage power MOSFETs:

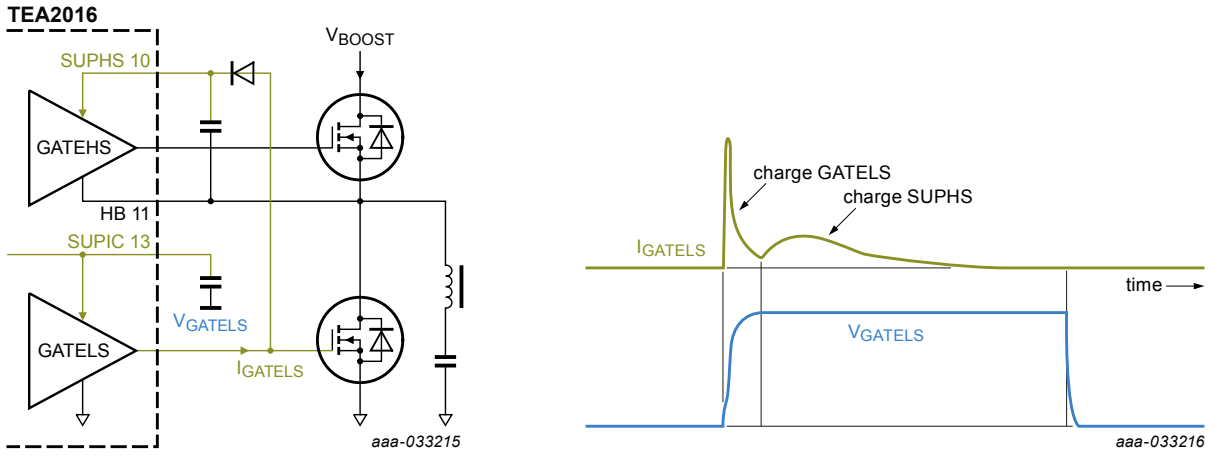
- GATEPFC for driving the PFC MOSFET
- GATELS for driving the low-side LLC MOSFET
- GATEHS for driving the high-side LLC MOSFET

7.1 GATEPFC

To drive the PFC high-voltage power MOSFET, the TEA2016AAT has a strong output stage.

7.2 GATELS and GATEHS

Both TEA2016AAT drivers have identical driving capabilities for the gate of an external high-voltage power MOSFET. The low-side driver is referenced to the GND pin and is supplied from the SUPIC pin. The high-side driver has a floating connection to the midpoint of the external half-bridge. It is referenced to HB. The high-side driver is supplied using a capacitor on the SUPHS pin. The capacitor is supplied using an external bootstrap function to the GATELS pin. When the low-side MOSFET is on and GATELS is high, the bootstrap diode charges C_{SUPHS}.



a. Circuit

b. Waveform

Figure 11. Supply system for GATELS and GATEHS

Both LLC drivers have a strong current source capability and an extra strong current sink capability. In general LLC operation, fast switch-on of the external MOSFET is not critical because the HB node swings automatically to the correct state after switch-off. Fast switch-off, however, is important to limit switching losses and prevent delay especially at high operating frequency.

7.3 General subjects on MOSFET drivers

7.3.1 Switch-on

The time to switch on depends on:

- The supply voltage for the internal driver
- The characteristic of the internal driver:
- Charging the gate capacitance
- The gate threshold voltage for the MOSFET to switch on
- The external circuit to the gate

7.3.2 Switch-off

The time to switch off depends on:

- The characteristic of the internal driver
- Discharging the gate capacitance
- The voltage on the gate just before discharge
- The gate threshold voltage for the MOSFET to switch off
- The external circuit to the gate

The internal driver can sink more current than it can source because the timing for switching off the MOSFET is more critical than the timing for switching it on. At higher frequencies and/or short on-time, timing becomes more critical for correct switching. Sometimes, a compromise between fast switching and EMI effects must be found. To optimize the switching behavior, a gate circuit between the driver output and the gate can be used.

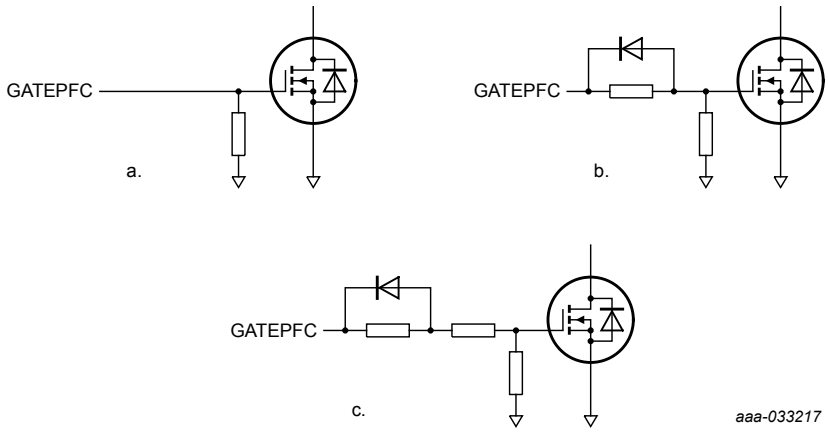


Figure 12. Examples of three different gate circuits

Switching on/off the MOSFETs using the drivers is approximated by alternating the charge and discharge of a MOSFET gate-source capacitance using a series resistor (representing the R_{DSon} of the internal driver MOSFET and connections). The resistor value for discharging is usually lower than for charging the gate.

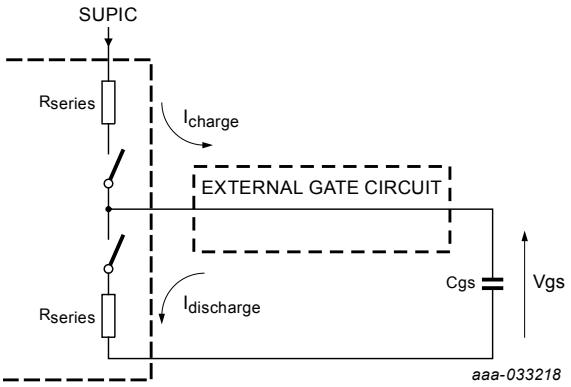


Figure 13. Simplified model of a MOSFET drive

7.4 Specification of the gate drivers

The main function of the internal MOSFET drivers is to source and sink current to switch on and off the external MOSFET. To show the capability of the internal driver, the amount of sink or source current is specified.

The simplified model in Figure 13 demonstrates that the charge and discharge current values depend on the supply and gate voltage conditions. When the supply voltage is highest and the gate voltage 0 V, the source current value is highest. When the gate voltage is highest, the sink current value is highest.

Table 2. Sink and source current specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GATELS AND GATEHS pins						
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 4 V	-	−340	-	mA
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{GND}$ = 4 V; V_{SUPIC} = 13 V	-	−340	-	mA
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 2 V	-	580	-	mA
		$V_{GATEHS} - V_{HB}$ = 11 V	-	2	-	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{GND}$ = 2 V; $V_{SUPIC} \geq$ 13 V	-	580	-	mA
		$V_{GATELS} - V_{GND}$ = 11 V; $V_{SUPIC} \geq$ 13 V	-	2	-	A
Gate driver output (GATEPFC)						
$I_{source(GATEPFC)}$	source current on pin GATEPFC	$V_{GATEPFC}$ = 2 V; $V_{SUPIC} \geq$ 13 V	-	−0.37	-	A
$I_{sink(GATEPFC)}$	sink current on pin GATEPFC	$V_{GATEPFC}$ = 2 V; $V_{SUPIC} \geq$ 13 V	-	0.36	-	A
		$V_{GATEPFC}$ = 10 V; $V_{SUPIC} \geq$ 13 V	-	1.4	-	A

7.5 Limiting values for the high-side driver GATEHS, SUPHS and HB

The high-side MOSFET driver for a half-bridge MOSFET stage has some specific behavior aspects because a circuit that is supplied by a “floating” supply drives it. The floating voltage SUPHS is supplied by a bootstrap circuit. The high-side MOSFET and the driver are referenced to the HB voltage node. Regarding the circuit ground level, the HB node continuously switches between (approximately) 0 V and input voltage (V_{boost}).

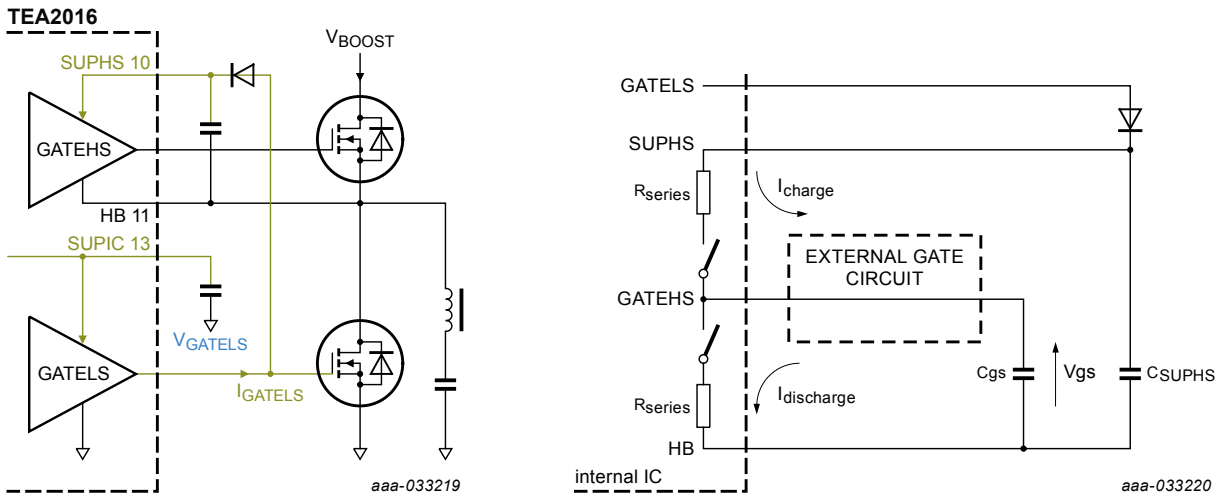


Figure 14. Supply system for GATEHS: GATELS charges SUPHS by bootstrap

7.5.1 Supply voltage for the GATEHS output driver: SUPHS

An external bootstrap buffer capacitor supplies the high-side driver. The bootstrap capacitor is connected between the high-side reference (the HB pin) and the high-side driver supply input (the SUPHS pin). An external diode from the GATELS pin charges this capacitor each time when HB is low.

Instead of using the GATELS pin as the power source for charging the SUPHS pin, another supply source can be used. In such a construction, it is important to check for correct start/stop sequences and to prevent that the SUPHS voltage exceeds 14 V (referenced to HB).

7.5.2 GATEHS switching

The simplified model in Figure 14 shows that when the external high side MOSFET is switched on, current is taken from SUPHS. The gate of the external MOSFET (that can be represented as a capacitor C_{gs}) is charged to a high voltage (V_{gs}) by switching on the internal high-side MOSFET. When the external MOSFET is switched off, the internal low-side MOSFET discharges C_{gs}.

The shape of the current is related to:

- The supply voltage for the internal driver (V_{SUPHS})
- The characteristic of the internal driver
- The gate capacitance to be charged
- The gate threshold voltage for the MOSFET
- The external circuit to the gate
- External parasitics

7.5.3 LLC circuit behavior and GATEHS

In Figure 15, the behavior of GATEHS has been split up into 6 events.

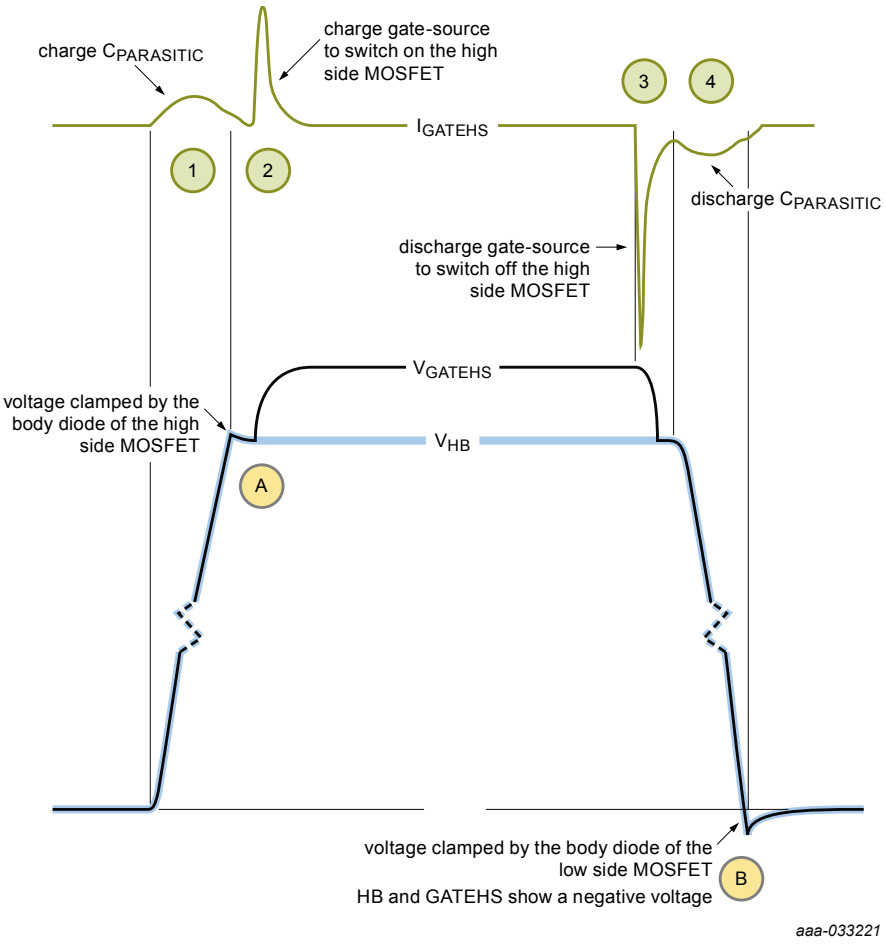


Figure 15. GATEHS current and voltage

Figure 16 and Figure 17 show the corresponding action in circuit diagrams that include the parasitic capacitance between GATEHS and ground.

1. During the positive HB slope, the internal lower MOSFET of GATEHS charges the parasitic capacitance.
2. During switch-on of the high-side LLC MOSFET, the charge current flows from SUPHS to the gate of the high-side LLC MOSFET through the internal upper MOSFET of GATEHS.
3. During switch-off of the high-side LLC MOSFET, the discharge current flows from the gate of the high-side LLC MOSFET to HB through the internal lower MOSFET of GATEHS.
4. During the negative HB slope, the conducting internal lower MOSFET of GATEHS discharges the parasitic capacitance.
5. At the end of the positive HB slope, the voltage on HB exceeds V_{BOOST}. The body diode of the high-side MOSFET clamps the voltage.
6. At the end of the negative HB slope, the voltage on HB becomes negative. The body diode of the low-side MOSFET clamps the voltage to ground level.

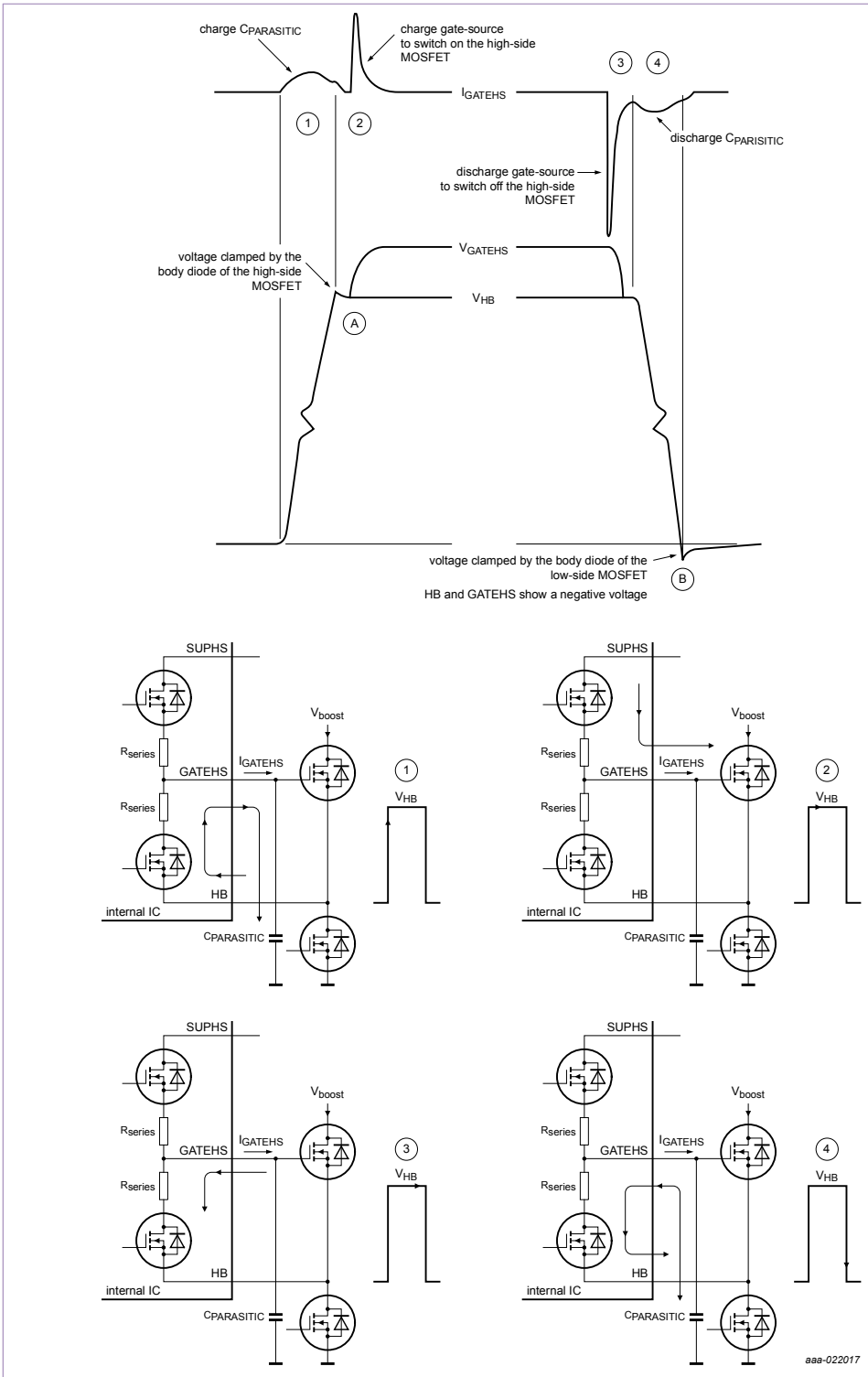


Figure 16. Current in GATEHS

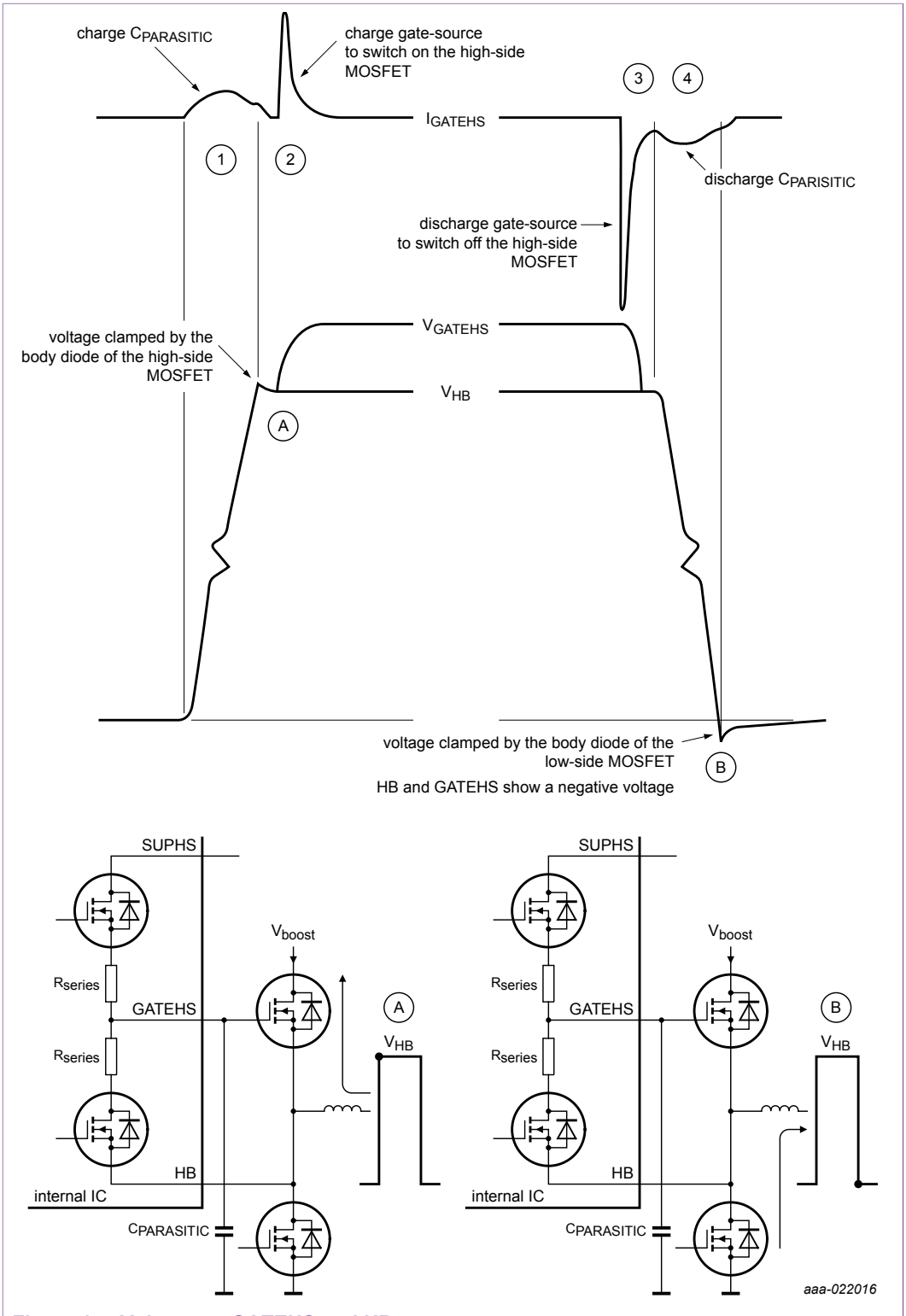


Figure 17. Voltage on GATEHS and HB

7.5.4 Limiting values SUPHS and HB

The HB node and the SUPHS node are closely related because the internal high-voltage circuit is supplied using the voltage between these nodes. The SUPHS voltage restrictions are related to the limits for the voltage on HB.

The values for HB can be derived from the voltage limits specified for SUPHS using the practical voltage between both nodes: V_{SUPHS} to V_{HB}.

Table 3. Limiting values defined for V_{SUPHS}, V_{HB}, and V_{GATEHS} in the data sheet

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{SUPHS}	voltage on pin SUPHS	during mains surge; t < 0.5 s; 10 times at a 0.1 Hz interval	−0.3	+685	V
		$V_{SUPHS} - V_{HB}$	−0.4	+13	V
V_{GATEHS}	voltage on pin GATEHS		$V_{HB} - 0.4$	$V_{SUPHS} + 0.4$	V
V_{HB}	voltage on pin HB	during mains surge; t < 0.5 s; 10 times at a 0.1 Hz interval	−3	+685	V
		t < 1 µs	−13	-	V

7.5.5 High dV/dt on HB and hard switching

In general, high HB dV/dt slopes must be prevented as they can cause disturbances in circuit parts.

Extra high dV/dt occurs during hard switching events:

- At start-up, when GATEHS is switched on and the HB voltage increases from 0 V to the input voltage.
- At the start of each burst, GATEHS is switched on and the HB voltage increases from approximately half the input voltage to the full input voltage.
- At the start of each LP cycle, GATEHS is switched on and the HB voltage increases from an HB ringing peak to the input voltage (see Section 9.5.1).

During these events, a higher value of the series resistor to the gate of the MOSFET for switch-on can limit the dV/dt. During normal zero voltage, switching the switch-on speed is not critical.

At very high HB dV/dt, the voltage level of GATELS and GATEPFC can drop because of internal circuit disturbances. For the MOSFET drive to be reliable during operation, this voltage drop must be avoided. The most critical condition to check is at LLC start-up (see Figure 18).

For a reliable operation, the GATELS output voltage must reach 9 V or higher during the on-time. At a lower voltage level, SUPHS supply via the bootstrap function and also the operation of the GATELS driver is endangered.

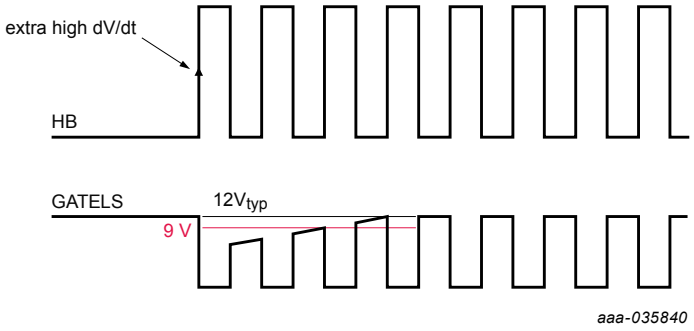


Figure 18. Too much GATELS voltage drop caused by a disturbance from a high HB dV/dt

7.5.6 GATEHS limits

7.5.6.1 GATEHS voltage

The GATEHS voltages remain approximately within the voltage between SUPHS and HB. In situation 1 (see Figure 15), the voltage on GATEHS can become a little lower than HB because of the conducting body diode. And at GATEHS switch off the voltage can become lower because of a ringing effect (seeTable 3 and Section 7.6).

7.5.6.2 GATEHS current

Measurement setup

The behavior of the current in GATEHS of a certain application can be checked in practice. Because the GATEHS current during the HB slopes is caused by charging/discharging the parasitic capacitance, increasing the parasitic capacitance a lot by the measurement setup must be avoided.

Do not connect a voltage probe because it adds a relatively high capacitance (on GATEHS for example).

A current probe is suitable for measurement because it normally adds only a little extra capacitance to the application circuit. Because of the little extra capacitance added by a current probe, the measurement results show higher currents than in the original circuit.

The extra current can be measured by (temporarily) adding a second current probe. Measuring the difference in current values between 1 probe connected and 2 probes connected, the additional current because of 1 probe can be found. Subtracting this probe-related current from the measurement result can provide more accurate values.

Current values

The SUPHS internal driver itself drives the currents in situation 2 and 3.

Another source causes the currents in situation 1 and 4. These currents must not become excessive. In situation 4, the GATEHS conducts to HB by the internal lower MOSFET of GATEHS. The peak current value is allowed to become similar to the discharge current without a problem. In situation 1, the GATEHS is not actively conducting but the current is flowing through the body diode of the internal lower MOSFET of GATEHS. The peak current level in situation 1 is normally much lower than the discharge current of the same lower MOSFET in situation 3.

The expected value by rule of thumb: $I_{peak\_in\_1} \approx -0.25 \times I_{peak\_in\_3}$.

At switch-off after situation 3, some parasitic ringing may occur. Section 7.6 provides a method to check this condition for the gate drivers in general.

7.6 Gate driver switch off and limiting values

Parasitic inductance in the IC-to-MOSFET connections leads to a ringing effect after switch off. A negative voltage and current occurs in the gate driver pin. PBC layout must be made such that long tracks are avoided. To prevent switching problems and to stay within specification of the IC function, the resulting behavior must be checked.

The limiting voltage values in the data sheet only provide a safe minimum DC level of −0.4 V. if the level is not very high and the duration is short, however, the internal driver circuit can handle some extra reverse current.

7.6.1 Method for determining if switch-off reverse current is still safe

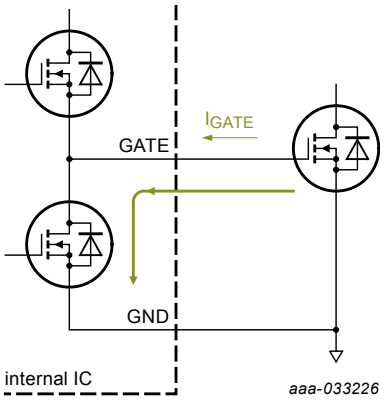
When a voltage measurement on the gate pin shows that the level is below −0.4 V, the current in the pin can be checked to judge the amount of energy in the IC gate drive circuit. Because of several parasitic elements in the gate drive circuit (application) and the IC, a voltage measurement is often not conclusive.

The gate current must be checked using a DC current probe and oscilloscope. Make sure that adding the current probe measurement does not (significantly) change the behavior of the circuit.

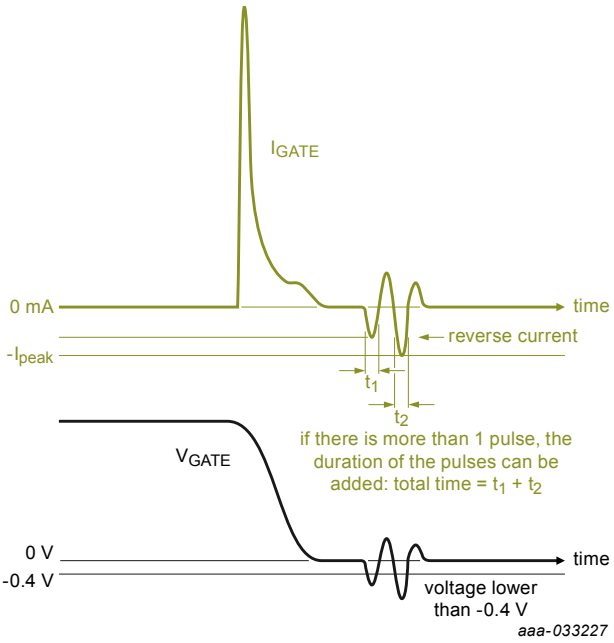
The reverse current is still safe when all three of the following conditions are met:

- The reverse current does not exceed −300 mA_{peak}
- The duration of one or more pulses is shorter than 500 ns in each event
- The repetition rate of the events is lower than 200 kHz

This rule is valid for GATELS, GATEHS, and GATEPFC.



a. Circuit



b. Timing diagram

Figure 19. Ringing after GATE driver switch off

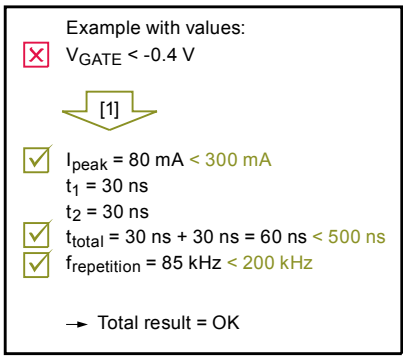


Figure 20. Example for checking if switch off the gate driver reverse current is OK

8 PFC functions

8.1 SNSMAINS: mains voltage sensing and OTP

The SNSMAINS pin combines two functions:

- The mains voltage sensing
- The sensing of an external NTC for detecting an over temperature protection (OTP)

The functions are alternatingly active in time.

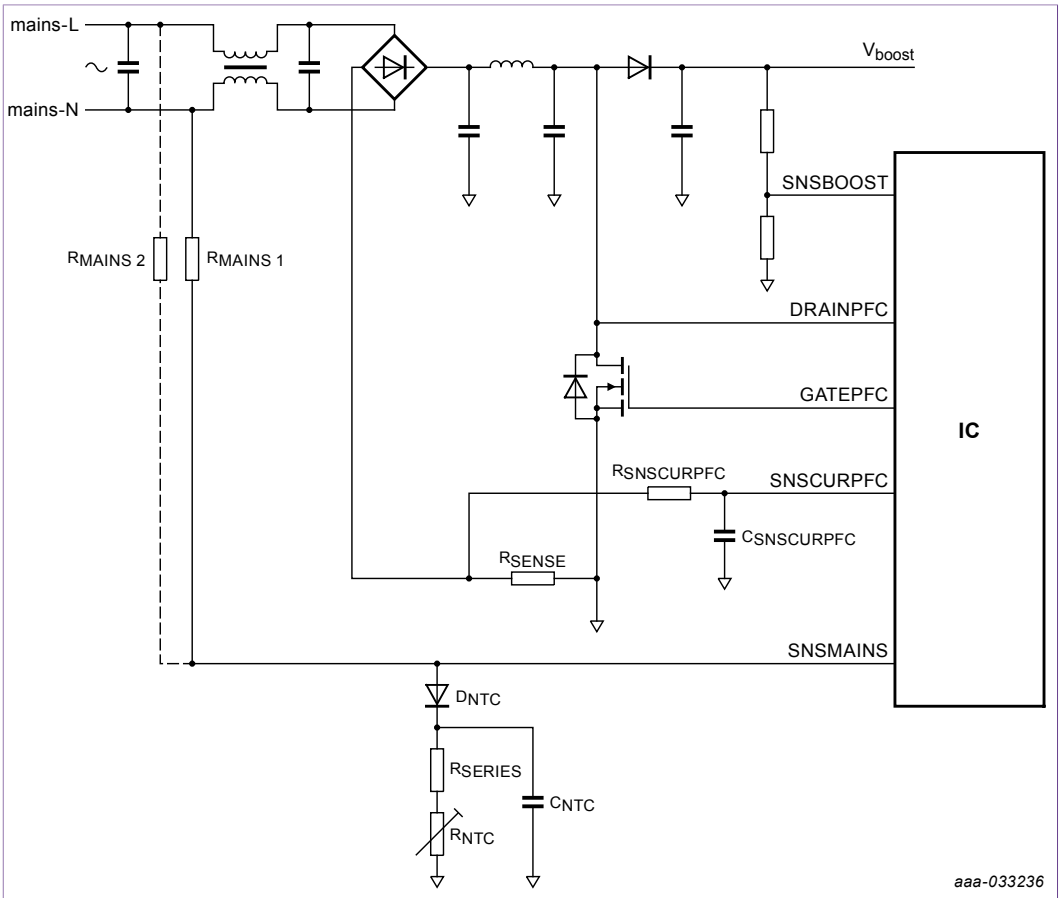


Figure 21. SNSMAINS: mains voltage sensing and OTP

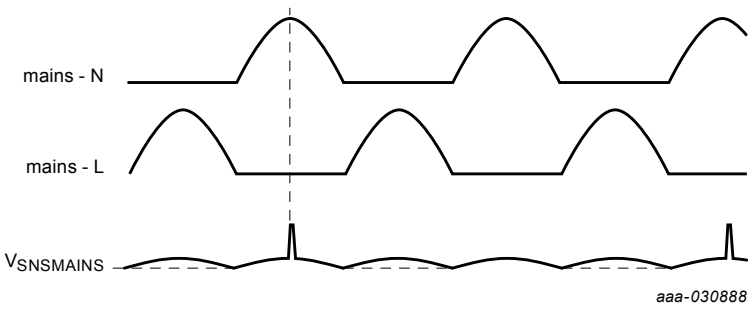


Figure 22. SNSMAINS: mains voltage sensing and OTP sensing in time

8.2 Mains voltage sensing by SNSMAINS

For mains sensing, the current flowing in the SNSMAINS pin is measured. The current depends on the external resistor value. A choice can be made to use 10 MΩ or 20 MΩ and to use 1 resistor to 1 mains connection or 2 resistors to both mains connections. Internally, the measurement resistor is selected to the correct value of 6 kΩ or 12 kΩ, in accordance with the parameter setting. During a half mains voltage cycle, the peak current value is determined and stored. The value is used as an input for:

- The mains compensation function of the PFC regulation loop
- The brownin and brownout function

At a selectable current level of 4.95 µA to 13.35 µA, the brownin level is reached and the IC starts switching. When the current drops to below the selectable hysteresis relative to the brownin level of 0.15 µA to 1.2 µA again, the brownout level is reached and the IC switching stops.

The selected current value sets an internal voltage level that triggers the brownin and brownout. The voltage level equals the current value multiplied by an internal 12 kΩ resistor. When using a system with a 6 kΩ resistor, the current from the mains is 2× the selected current value setting.

When, after brownout, the brownin level is reached again, a latched protection state is reset.

If during a selectable delay of 100 ms to 400 ms mains is not detected, the X-capacitor discharge function is activated. During the X-capacitor discharge mode, the SNSMAINS current is monitored for reconnecting the mains again. Selecting the infinite delay option, disables the X-capacitor discharge function.

8.2.1 Using two resistors for mains voltage sensing

When using two sensing resistors, the currents from both mains connections are added. One of the two currents is often zero and the result is correct. But sometimes, neither current is zero. The resulting SNSMAINS measurement is higher than in reality then. If this situation provides problems, it can be improved by adding a series diode to both resistors to ensure that SNSMAINS only measures the voltage from the highest voltage connection.

8.3 SNSMAINS brownin and brownout

At a selectable current level of 4.95 µA to 13.35 µA, the brownin level is reached and the IC starts switching. When the current drops to below the selectable hysteresis relative to the brownin level 0.15 µA to 1.2 µA again, the brownout level is reached and the IC switching stops.

When, during PFC operation, the current level drops to below the selected mains brownout level, an internal timer of a selectable brownout delay valued 25 ms to 1200 ms is started. The current level must remain below the brownout level during this period before the brownout protection is activated.

At brownout, the PFC operation is stopped. There is also an option to stop the LLC operation after a selectable disable LLC at the end of a brownout detection delay time ranging between 125 ms to 6000 ms. When the value is set to off, the LLC remains operating.

Example:

$V_{mains(peak)} = 1.41 \times V_{mains(rms)}$

$I_{brownin} = 5.7\ \mu A$

Brownout hysteresis = 0.75 µA → $I_{bo} = 4.95\ \mu A$

$R_{SNSMAINS} = 20\ M\Omega$

$R_{SNSMAINS(int)} = 12\ k\Omega$

$V_{bi(rms)} = 1 / 1.41 \times (I_{bi} \times (R_{SNSMAINS} + R_{SNSMAINS(int)})$
$= 1 / 1.41 \times (5.7\ \mu A \times (20\ M\Omega + 12\ k\Omega)) = 80.9\ V$

$V_{bo(rms)} = 1 / 1.41 \times (I_{bi} \times (R_{SNSMAINS} + R_{SNSMAINS(int)}) =$
$1 / 1.41 \times (4.95\ \mu A \times (20\ M\Omega + 12\ k\Omega)) = 70.3\ V$

8.4 NTC measurement for external OTP on SNSMAINS

The OTP measurement is done at the top of the mains voltage, just after the mains measurement has finished the peak detection. During 50 µs a selectable current between 150 µA and 1050 µA flows from the pin through the external diode and NTC to ground. The resulting voltage on pin is measured. When the voltage on the pin is below 3 V during a selectable time of between 0.5 s and 8 s, the OTP protection is activated.

The protection value of the NTC can be calculated like in this example:

$R_{NTC} = (V_{det(SNSMAINS)} - V_{forward\_diode}) / I_{o(SNSMAINS)} - R_{series} =$
$(3\ V - 0.6\ V) / 300\ \mu A - 3.3\ k\Omega = 4.7\ k\Omega$

With the required temperature level and the calculated NTC value, a suitable device can be selected. To optimize the protection function with the selected NTC type, the R_{series} value can be modified.

Setting the current level to 0 µA disables the external OTP function. When the function is not required, the NTC circuit components can be omitted.

The series diode prevents mutual influence of the mains sensing and the OTP measurement. The diode type must be a low-current leakage type, for example, BAS416.

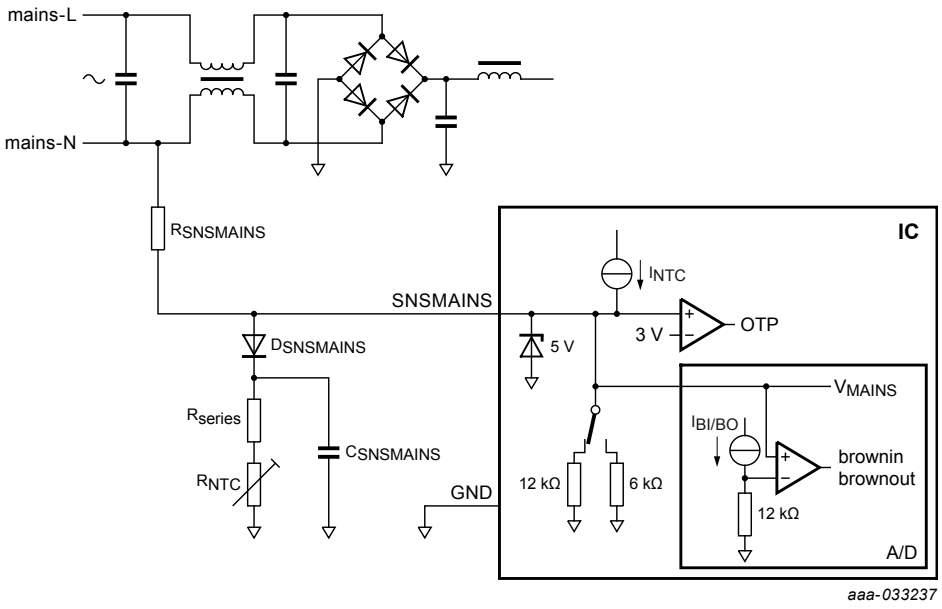


Figure 23. Typical external OTP function implementation on SNSMAINS with NTC

8.5 PFC operation

The PFC operates in quasi-resonant (QR) or discontinuous conduction mode (DCM) using valley detection to reduce the switch-on losses. The maximum switching frequency of the PFC is limited to a selectable PFC maximum switching frequency of between 75 kHz and 500 kHz. Valley skipping lowers the frequency limit, which reduces switching losses. The reduction of switching losses is mainly near the zero-voltage crossings of the mains voltage. It is very effective at medium/low output load condition.

The PFC is designed as a boost converter with a fixed output voltage. An advantage of a fixed boost converter is that the LLC can be designed to a high input voltage, making the LLC design easier. Another advantage of the fixed boost is the possibility of using a smaller boost capacitor value or having a significantly longer hold-up time.

In the TEA2016AAT system, the mains sensing is always active. When the mains voltage is present, the PFC is switched on first. When the boost capacitor is close to its nominal value ($V_{SNSBOOST}$ = 2.5 V), the LLC is switched on (LLC brownin).

For improved efficiency at low output loads, the system can be operated in burst mode. During burst mode, the LLC burst situation controls the activation and deactivation of the PFC burst mode based on the LLC BM duty cycle. The PFC can be set to operate BM independently or synchronized with the LLC burst.

During development work, a PFC operation setting can temporarily disable the PFC operation.

8.6 PFC output power and peak current

The PFC of the TEA2016AAT is on-time controlled. So, measuring the mains phase angle is not required. To obtain a good power factor (PF) and mains harmonics reduction (MHR), the on-time is kept constant during the half sine wave for a given mains voltage and load condition.

When the on-time is constant, the PFC input peak current level follows the shape of the mains voltage. To obtain this behavior, the on-time regulation during load variations is slow.

An essential parameter for the PFC coil design is the highest peak current. This current occurs at the lowest input voltage at maximum power.

The maximum peak current $I_{p(max)}$ for a PFC operating in critical conduction mode can be calculated with Equation 1.

$$I_{p(max)} = \frac{2\sqrt{2} \times P_{i(max)}}{V_{min}(AC)} = \frac{2\sqrt{2} \times \frac{P_{o(nameplate)}}{\eta}}{V_{min}(AC)} \quad (1)$$

Example:

- Efficiency (η) = 0.9
- $P_{o(nameplate)}$ = 250 W
- V_{min} (AC) = 90 V

$I_{p(max)}$ = 8.73 A

$I_{p(max)}$ + 10 % = 9.60 A

The TEA2016AAT PFC operates in quasi-resonant (QR) mode with valley switching providing good efficiency. Valley detection requires additional ringing time within every switching cycle. This ringing time adds short periods of no-power transfer to the output capacitor. The system must compensate this using a higher peak current. A rule of thumb is that the peak current in QR mode is maximum 10 % higher than the calculated peak current in critical conduction mode.

8.7 PFC output voltage regulation SNSBOOST

A resistive divider between the PFC output voltage, the SNSBOOST pin, and GND sets the boost output voltage. When in regulation, the SNSBOOST voltage is kept at 2.5 V.

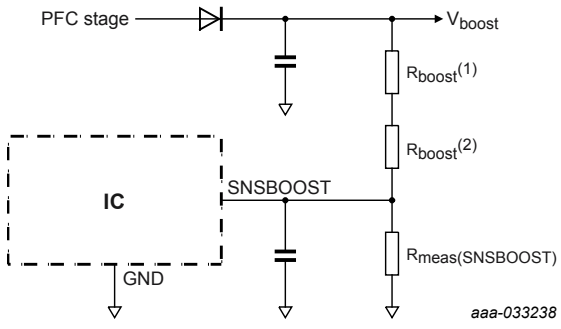


Figure 24. PFC output regulation by SNSBOOST

The value of the resistors between the PFC output voltage and the SNSBOOST pin can be calculated with Equation 2:

$$R_{boost} = R_{boost1} + R_{boost2} \quad (2)$$

$$R_{boost} = R_{measure(SNSBOOST)} \times \frac{V_{boost} - V_{reg(SNSBOOST)}}{V_{reg(SNSBOOST)}}$$

Typical system values are:

- $R_{measure(SNSBOOST)}$ = 100 kΩ
- $V_{reg(SNSBOOST)}$ = 2.5 V

Example:

To obtain a nominal PFC output voltage of V_{boost} = 390 V, R_{boost} must be 15.6 MΩ.

8.8 PFC gate driver GATEPFC

The circuit driving the gate of the power MOSFET has a high current sourcing capability $I_{source(GATEPFC)}$ of 0.37 A. It also has a high current sink capability $I_{sink(GATEPFC)}$ of 1.4 A. The source and sink capabilities allows fast switch-on and switch-off of the external power MOSFET to ensure efficient operation. The driver is supplied from SUPIC via an internal voltage regulator to ensure a drive voltage of 12 V.

Do not use active components, like transistors, in the gate drive circuit to enhance switching behavior. They introduce a risk of bad switching behavior in special conditions.

8.9 PFC on-time control

The PFC operates by on-time control. The following determine the PFC MOSFET on-time:

- The voltage on SNSBOOST to be regulated to 2.5 V.
- Mains compensation using the mains voltage values sensed by SNSMAINS.
- Option for Power Factor improvement that modulates the on-time within the 2nd half of the half mains cycle. See Section 16.4.

In the TEA2016AAT, the loop control is digitally implemented and behaves as the diagram in Figure 25.

The error amplifier gain function is non-linear. When the SNSBOOST voltage deviation from 2.5 V is greater, the gain is higher. The higher gain provides a faster reaction at a load step. However, it can also show a longer output voltage settling time at start-up.

The PFC gain setting (0.25 to 1) can modify the general gain.

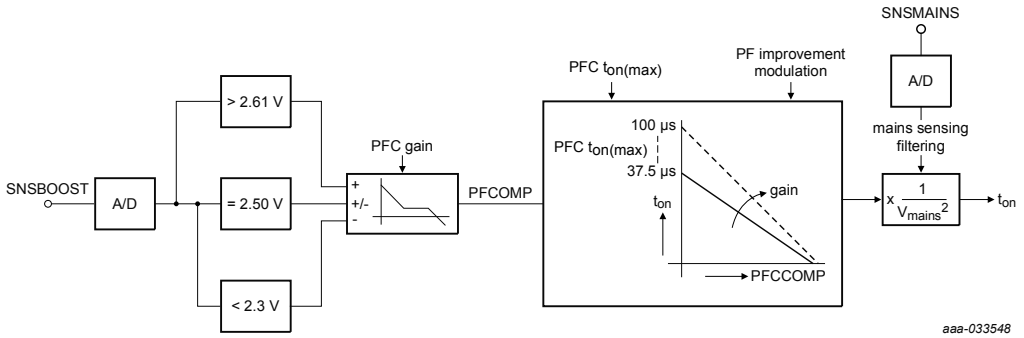
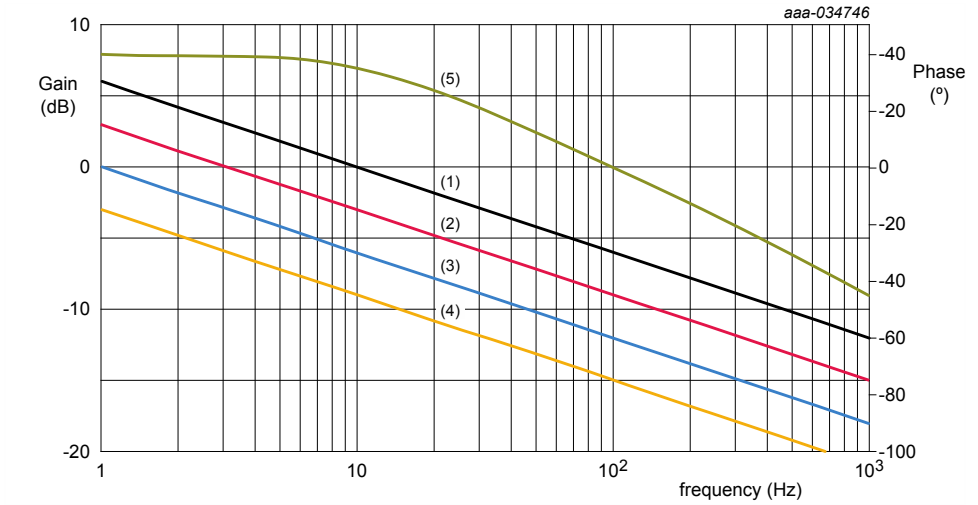


Figure 25. PFC loop control by t_{on}

The PFC gain setting (0.25 to 1) can modify the general gain.



(1) PFC gain = 1
(2) PFC gain = 0.75
(3) PFC gain = 0.5
(4) PFC gain = 0.25
(5) PFC gain = phase

Figure 26. Typical PFC gain-phase plot with different PFC gain settings

The PFC t_{on} maximum setting, 37.5 µs to 100 µs can modify the maximum on-time.

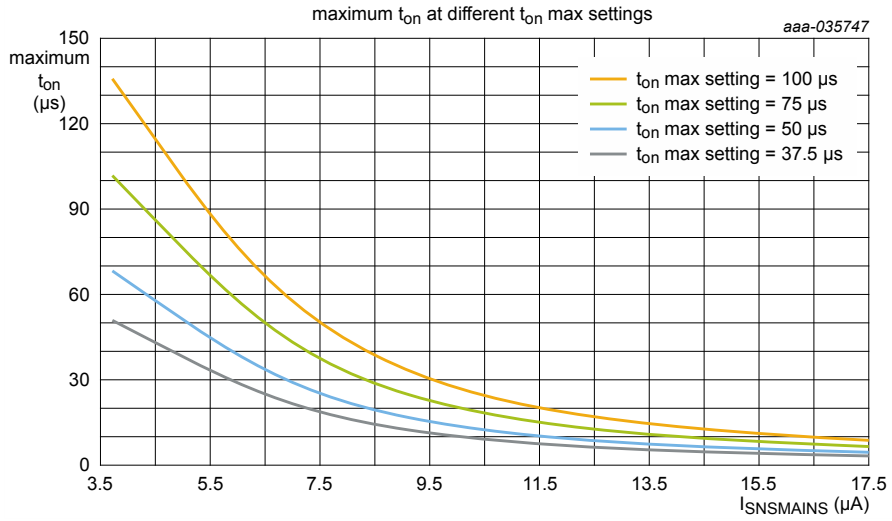


Figure 27. Maximum on-time different value settings as a function of mains values

8.10 Mains compensation in the PFC voltage control loop

The PFC transfer function from which the PFC on-time can be derived is inversely proportional to the squared mains input voltage.

$$K\left(V_{mains}\right) = \frac{A}{V_{mains}^{2}} \tag{3}$$

In a typical application, the result is a low bandwidth for low mains input voltages. And at high mains input voltages, the MHR requirements can be hard to meet.

The TEA2016AAT contains a correction circuit to compensate for the mains input voltage influence. The peak mains voltage is measured at the SNSMAINS pin and used for the internal compensation. Figure 25 shows the implementation on block level.

Using this compensation, it is possible to keep the regulation loop bandwidth constant over the complete mains input voltage range. This compensation also yields a fast transient response on load steps, while still complying with class-D MHR requirements.

When the mains voltage changes, this compensation changes the PFC on-time. To avoid variations of the on-time because of disturbances, a stable mains voltage measurement on SNSMAINS is required. Because an ADC function in the IC senses the mains voltage, there are discrete threshold levels of modifying the compensation. Near a threshold level, the system is sensitive to disturbances, which change the on-time. If disturbances occur, extra mains filtering can be considered. Figure 28 shows an example. Make sure that the filter reduces the higher (disturbance) frequencies and does not give distortion of the mains signal itself.

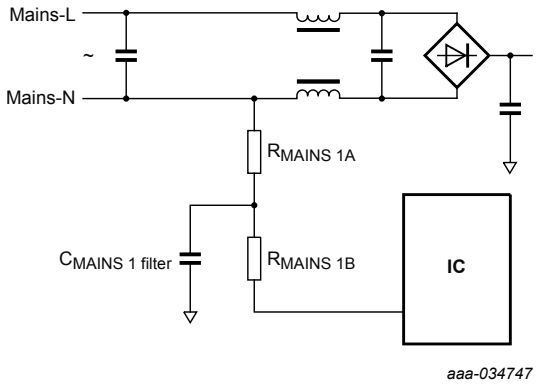


Figure 28. Reducing disturbance on SNSMAINS by adding a filter capacitor

8.11 PFC soft start at start-up

To prevent audible transformer noise at start-up, an internal soft start function slowly increases the on-time.

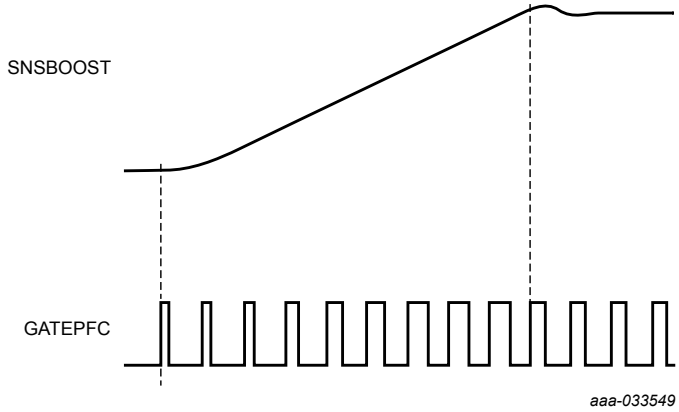


Figure 29. PFC soft start at start-up

8.12 PFC demagnetization sensing by SNSCURPFC

To ensure that the TEA2016AAT operates in discontinuous or quasi-resonant mode, the PFC MOSFET is switched on after the PFC coil is demagnetized. To reduce switching losses and electromagnetic interference (EMI), the next stroke is started when the PFC MOSFET drain-source voltage is at its minimum (valley switching). The demagnetization and valley detection are measured via the SNSCURPFC and the DRAINPFC pin.

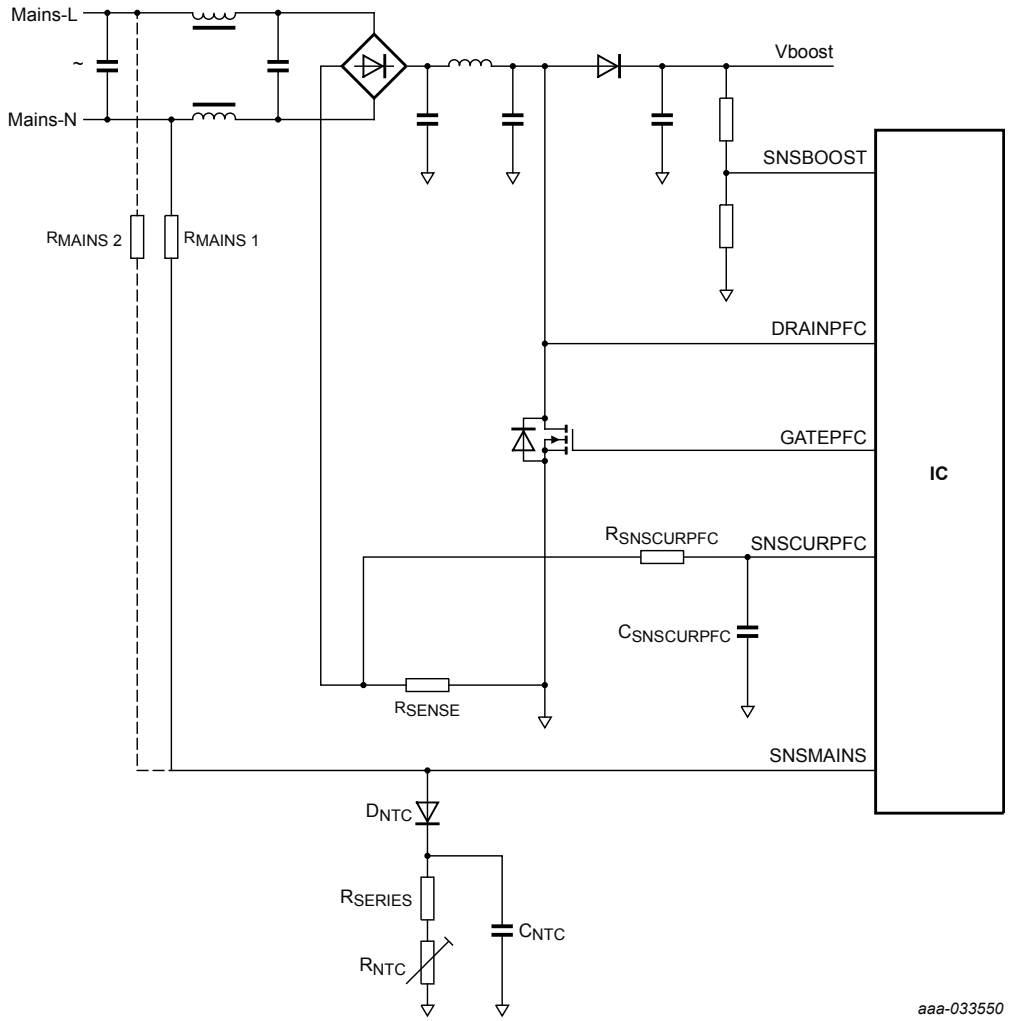


Figure 30. TEA2016AAT PFC application

The SNSCURPFC detects the PFC current by the voltage over measurement resistor R_{SENSE}. When the voltage has increased to above −10 mV, demagnetization is detected on the SNSCURPFC pin.

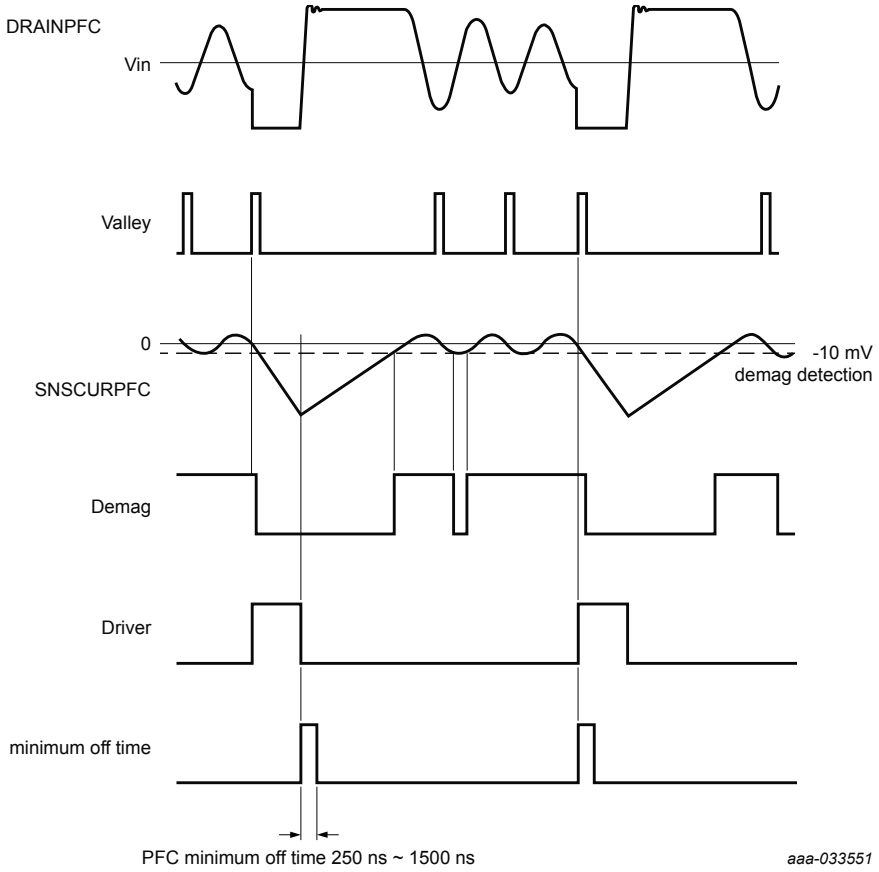


Figure 31. PFC converter state sensing by DRAINPFC and SNSCURPFC

8.13 SNSCURPFC filter

For suppressing voltage ringing because of disturbances and parasitic elements in the sensing circuit, a filter must be added (see Figure 30: $R_{SNSCURPFC}$ and $C_{SNSCURPFC}$).

For protecting the IC during events that make a serious negative voltage across R_{SENSE} at connecting the mains voltage or mains surge testing, the value of $R_{SNSCURPFC}$ series resistor must be 100 Ω or higher. The series resistor limits the current for an internal voltage limiting circuit.

The value of $C_{SNSCURPFC}$ is 2.2 nF typical. It must be connected close to the IC. To reduce the high-frequency disturbing signals but keep the current sensing signal unaffected, the value can be selected experimentally.

8.14 PFC minimum off-time

After the PFC MOSFET is switched off, there is a short time that the MOSFET cannot be turned on again. This function prevents that the MOSFET can turn on immediately after switch-off because of false triggering of events (disturbance signals). The PFC minimum off-time setting, 250 ns to 1500 ns can select the duration of this time.

8.15 PFC valley sensing at DRAINPFC

If the voltage at the MOSFET drain is at its minimum (valley), the PFC MOSFET is switched on for the next stroke. This action reduces switching losses and EMI (see Figure 31).

The internal valley sensing function on the DRAINPFC pin detects the valleys.

If no valley is detected within a selectable PFC maximum ringing time value between 5 µs to 20 µs after demagnetization, the MOSFET is forced to switch on.

8.16 PFC frequency limiting

To minimize PFC MOSFET switching losses, the switching frequency is limited to $f_{sw(PFC)max}$.

If the switching frequency for quasi-resonant operation exceeds the $f_{sw(PFC)max}$ limit, the system enters Discontinuous Conduction Mode (DCM). In general, the PFC MOSFET switches on at a minimum voltage across the switch (valley switching). To limit the switching frequency when the maximum frequency value is reached, the system starts skipping valleys (switching on at the next valley).

The maximum switching frequency value can be selected.

Power factor, THD, and efficiency

The PFC maximum switching frequency and the Ton increase function can be used to reduce THD (harmonic distortion) and increase the Power Factor. A higher value for the PFC maximum switching frequency improves the power factor and the THD. However, it reduces the efficiency at lower load conditions (and high mains voltage).

8.17 PFC overcurrent regulation OCR at SNSCURPFC

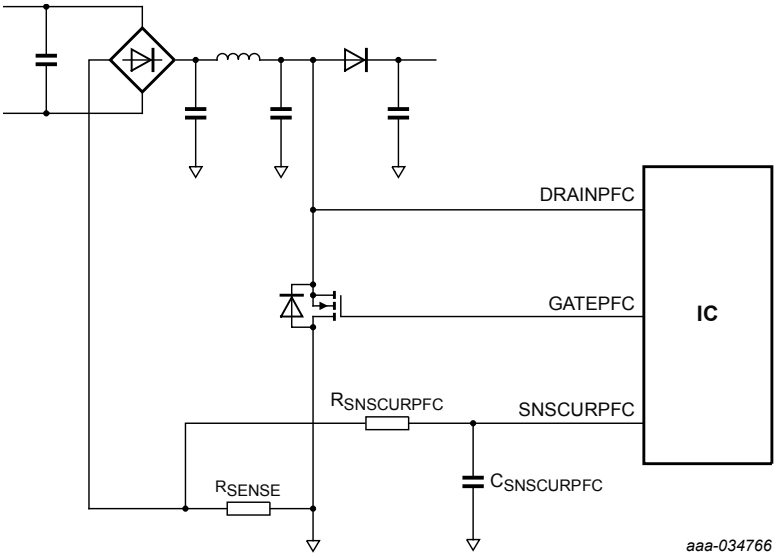


Figure 32. SNSCURPFC senses the PFC current

The maximum PFC peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor in series with the mains bridge rectifier. The result is a negative voltage regarding the ground of the IC. The voltage is measured via

the SNSCURPFC pin of the TEA2016AAT and is limited to −300 mV. When the SNSCURPFC voltage reaches −300 mV, the MOSFET is switched off.

For design, it is advised to include a margin of approximately 30 mV (10 %) for the value of the measurement resistor to compensate for practical deviations.

Example:

$R_{SENSE} = (V_{ocr(SNSCURPFC)} – 30\ mV) / I_{p,max} = (300\ mV – 30\ mV) / 8.73\ A_p = 28\ m\Omega$

During a switching cycle, a voltage peak appears on the SNSCURPFC pin when the PFC MOSFET is switched on due to the discharging of the MOSFET drain capacitance. The leading-edge blanking time of a selectable PFC OCP blanking time value between 200 ns to 500 ns ensures that the overcurrent sensing function does not react to this peak.

8.18 Active X-capacitor discharge

The TEA2016AAT provides an active X-capacitor discharge function by switching the internal HV current source on DRAINPFC to GND.

To suppress electromagnetic interference in most applications, a filter is required on the mains input. In addition to an inductance, EMI filters typically include one or more X-capacitors connected between the mains input terminals.

The active X-capacitor discharge function reduces the voltage between the device mains terminals to a safe value within a certain time period after the device is disconnected from the mains. In some regulatory regimes, this reduction is mandatory. If the voltage is not reduced, there is a risk of electrical shock by inadvertently contacting the terminals of the plug.

In most applications, resistors between the mains connections provide this function. This resistive path always takes some power from the mains during operation. In the TEA2016AAT concept, these resistors are not needed. To limit circuit current consumption during operation, the TEA2016AAT activates the discharge function only when it is needed. It improves the no load and low load power consumption performance.

The SNSMAINS mains sensing function monitors the input voltage every cycle. When a mains disconnection is detected, the HV current source on DRAINPFC is activated and switched to GND to discharge the X-capacitors and additionally also the output capacitor of the bridge rectifier.

X-capacitor discharge delay time after AC-off

If during a selectable delay of 100 ms to 400 ms no mains voltage is detected, the X-capacitor discharge function is activated. During the X-capacitor discharge mode, the SNSMAINS current is monitored for reconnecting the mains again. The X-capacitor discharge function can be disabled by selecting the infinite delay option.

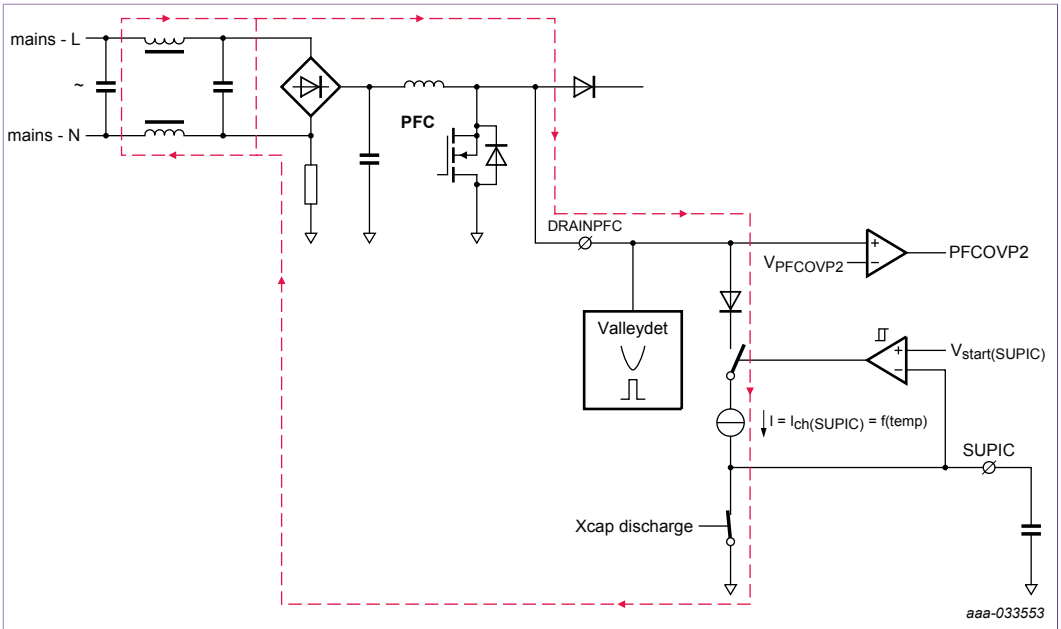


Figure 33. X-capacitor discharge by DRAINPFC current source switched to GND

The delay time between mains switch-off and activating the X-capacitor discharge function does not depend on the setting for mains brownout delay time to stop PFC operation.

At high load operation and medium load operation, the PFC operation quickly discharges the X-capacitor. The active X-capacitor discharge function is useful at a low-load condition or a no-load condition when the PFC operation (in BM) does not discharge the X-capacitor sufficiently.

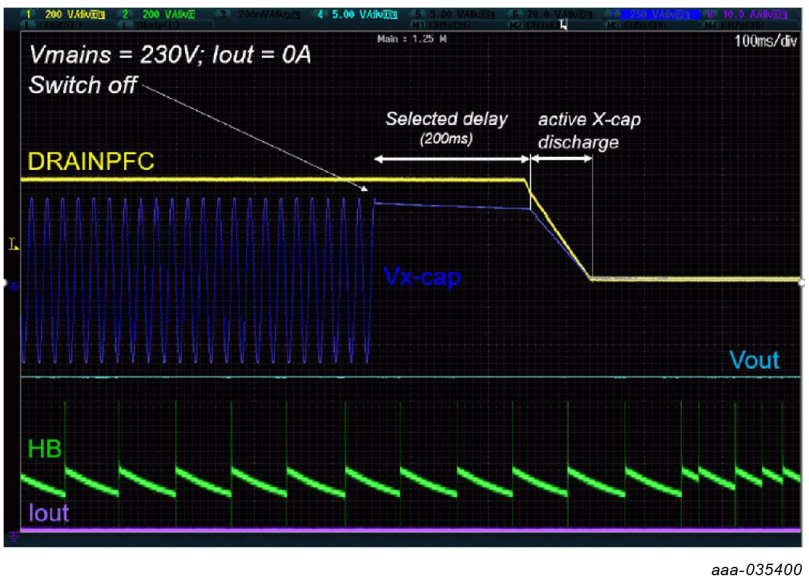


Figure 34. X-capacitor discharge at no-load condition when operating in burst mode

8.19 PFC burst mode

The system can be operated in burst mode for improved efficiency at low output loads. During burst mode, the LLC burst situation controls the activation and deactivation of the PFC burst mode based on the LLC BM duty cycle.

The PFC enters burst mode when the LLC is in burst mode and the LLC burst duty cycle is below 50 %. When the LLC is out of burst mode or the LLC burst duty cycle exceeds 75 %, it leaves burst mode.

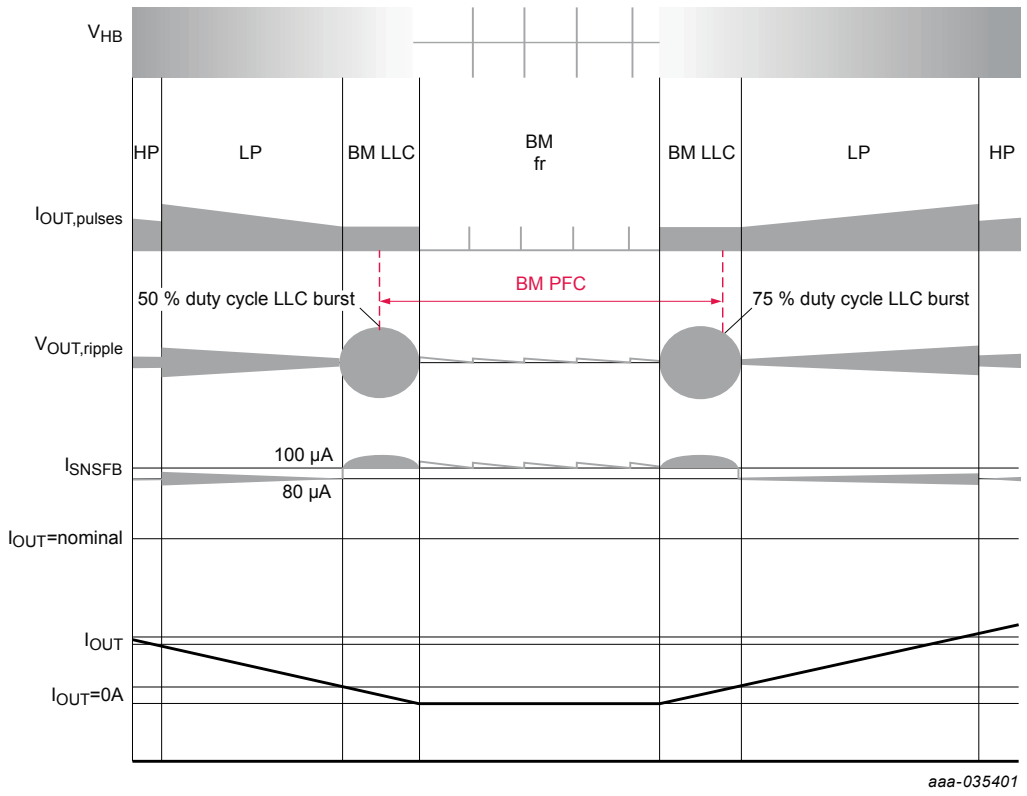
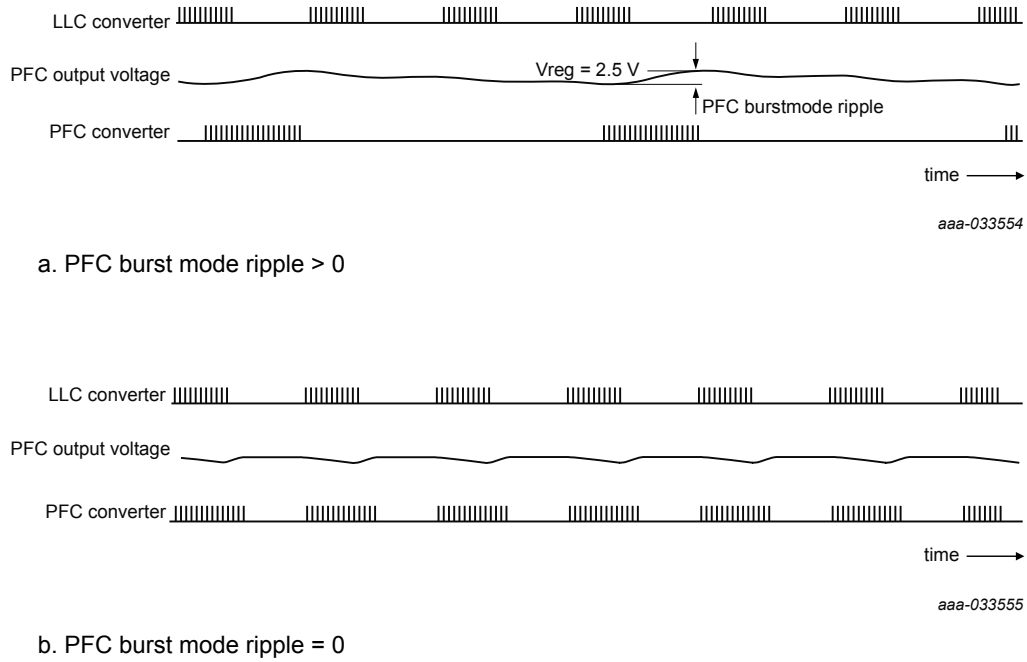


Figure 35. PFC enters BM at LLC burst-dc = 50 % and leaves at LLC burst-dc = 75 %

The PFC can be set to operate BM independently or synchronized with the LLC burst. The PFC burst mode SNSBOOST ripple setting can select the type.



a. PFC burst mode ripple > 0

b. PFC burst mode ripple = 0

Figure 36. PFC burst independently by output voltage hysteresis or synchronized with LLC

PFC burst mode by output voltage ripple

The parameter PFC burst mode SNSBOOST ripple can set the value for the PFC output voltage ripple.

When the PFC output voltage drops below this level, the PFC starts switching. When it reaches the regulation level again, it stops switching.

A higher voltage ripple value reduces the power consumption at (very) low load conditions. But it decreases the PFC performance on reaction time.

PFC burst mode synchronous with LLC burst

When the PFC burst mode SNSBOOST ripple value is set to zero, the PFC starts switching as soon as the LLC starts switching for a next burst. When the output voltage reaches the regulation level and the LLC stops switching, it stops.

This type of PFC burst mode operation results in less reduction of the power consumption compared to type with a high output voltage ripple value. But it provides more stable and responsive converter operation.

PFC burst mode soft start and soft stop

To reduce the audible noise, a soft start and/or a soft stop can be added to the PFC burst. These functions can be activated by setting a selectable value for the soft start/stop duration.

The PFC on-time is increased (soft start) or reduced (soft stop) during the selected time. The selected value (short, normal, or long) is just an indicator for the duration of the resulting soft start/stop behavior, because the normal PFC regulation is active during this period and strongly influences the on-time.

PFC on-time regulation in BM

PFC regulation is very slow during no-load conditions or very low-load conditions. The normal on-time regulation is only active during the bursts. When the IC is in energy save state, it is on hold during the periods between the burst.

9 LLC functions

9.1 LLC start and SNSBOOST UVP

After the SUPIC start level is reached and the initial procedures are completed, the LLC converter starts operation when the input voltage is higher than a selectable level that is close to the nominal boost voltage to ensure proper working of the LLC: SNSBOOST = 2.1 V to 2.4 V

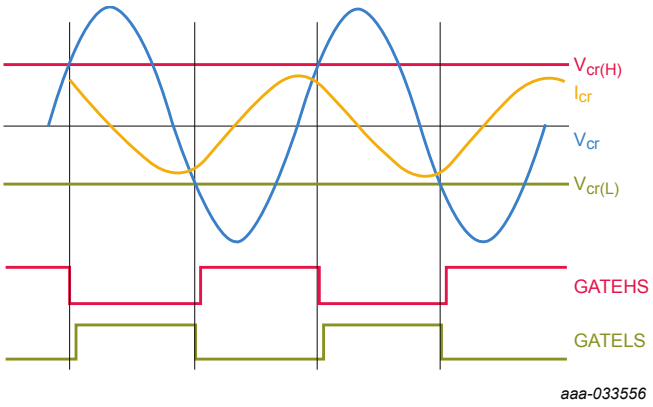
The voltage on the SNSBOOST pin is sensed continuously. When the voltage on SNSBOOST drops below a selectable low level (1 V to 2.05 V), switching of the LLC is stopped when the low-side MOSFET is on. When the SNSBOOST voltage exceeds the selected start level, the LLC (re)starts.

9.2 Power regulation by VCAP control

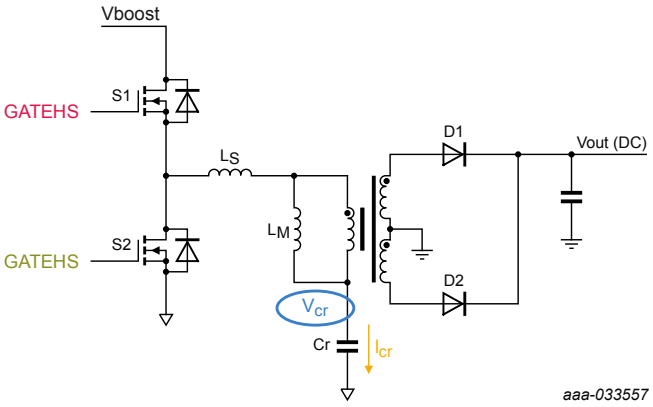
To control the output power, the TEA2016AAT uses the voltage across the resonant capacitor (V_{CAP}). V_{CAP} has a linear relationship with the output power. The voltage changes on the resonant capacitor are the result of the primary current that drives the power conversion.

Switching off the gate drive at a certain voltage on V_{CAP} controls the power. The adaptive non-overlap function drives the gate drive switch-on.

The system feedback drives the V_{CAP} levels for higher or lower power.



a. Signals in time



b. Circuit

Figure 37. V_{CAP} power control: switch off at the required V_{CAP} voltage level ($V_{cr(H)}$ and $V_{cr(L)}$)

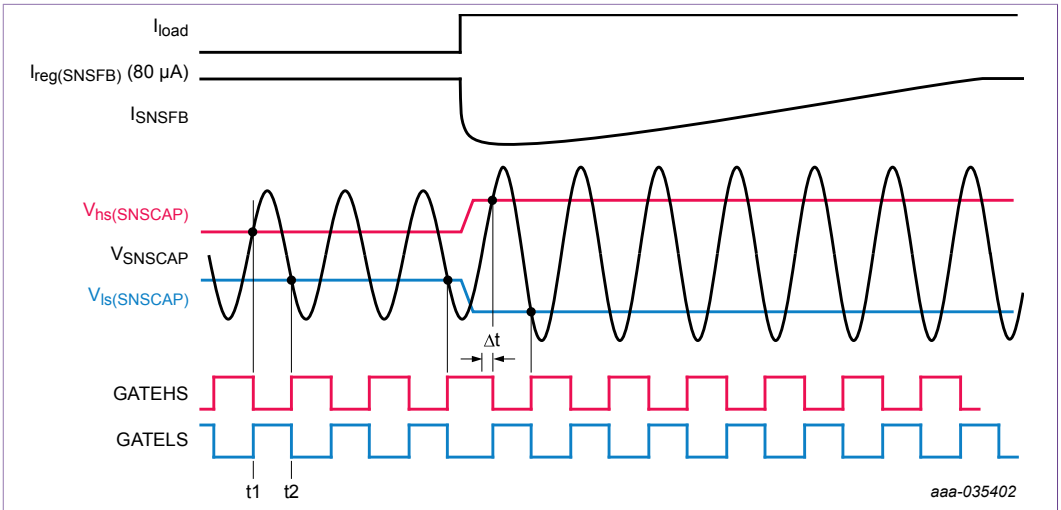


Figure 38. Example of changing VCAP levels ($V_{cr(H)}$ and $V_{cr(L)}$) at increasing output power

9.2.1 Sensing V_{CAP} by capacitive and resistive divider

A capacitive divider on SNSCAP senses the voltage on the resonant capacitor. In parallel, a resistive divider provides DC information. It is important that the shape of the signal is not distorted.

9.2.2 Scaling the V_{CAP} range to SNSCAP

The values of the divider must scale the voltage range for the output power onto the available 3 V range on SNSCAP. Because SNSCAP is internally biased to 2.5 V, the minimum voltage on SNSCAP is 1 V and the maximum voltage on SNSCAP is 4 V.

The used range during normal operation is much smaller because the V_{CAP} control uses input voltage compensation and a power range of 200 % power.

At nominal input voltage ($V_{SNSBOOST}$ = 2.5 V) and nominal (100 %) output power $V_{cr(H)}$ = 3 V and $V_{cr(L)}$ = 2 V.

$$V_{cr(H)} = 2.5 + \left(\frac{1.6\ V}{V_{SNSBOOST}} \times 0.0075\ \ V \times P_{out\%}\right) \quad (4)$$

$$V_{cr(L)} = 2.5 - \left(\frac{1.6\ V}{V_{SNSBOOST}} \times 0.0075\ \ V \times P_{out\%}\right) \quad (5)$$

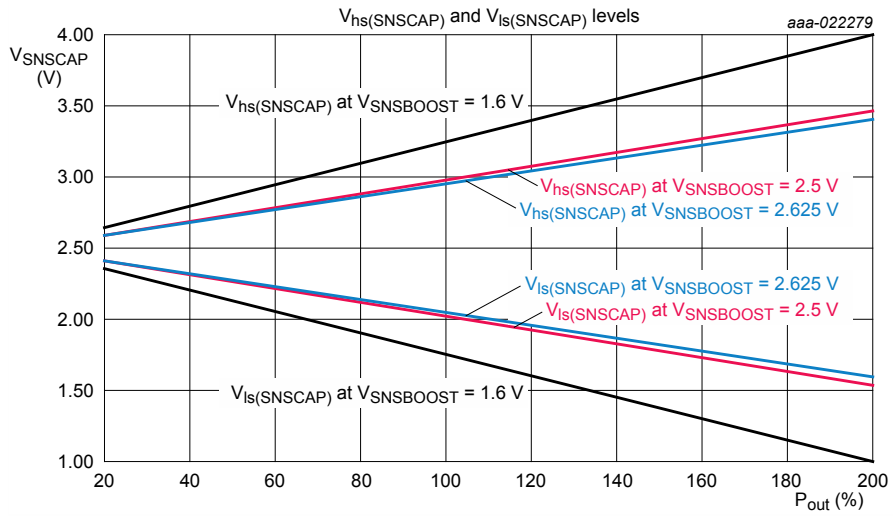


Figure 39. V_{cap} control: $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ levels on V_{SNSCAP}

In practice, the converter regulation SNSFB corrects any deviations in the regulation chain. The actual $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ levels may deviate a little from the ideal values used for the nominal design.

The levels in Figure 39 are valid for the HP mode. Below, a preset power level the LP mode is entered and the levels are recalculated to fit the correct $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ LP levels for operation.

9.2.3 Calculation of the SNSCAP divider value: CSNSCAPlow and CSNSCAPhigh

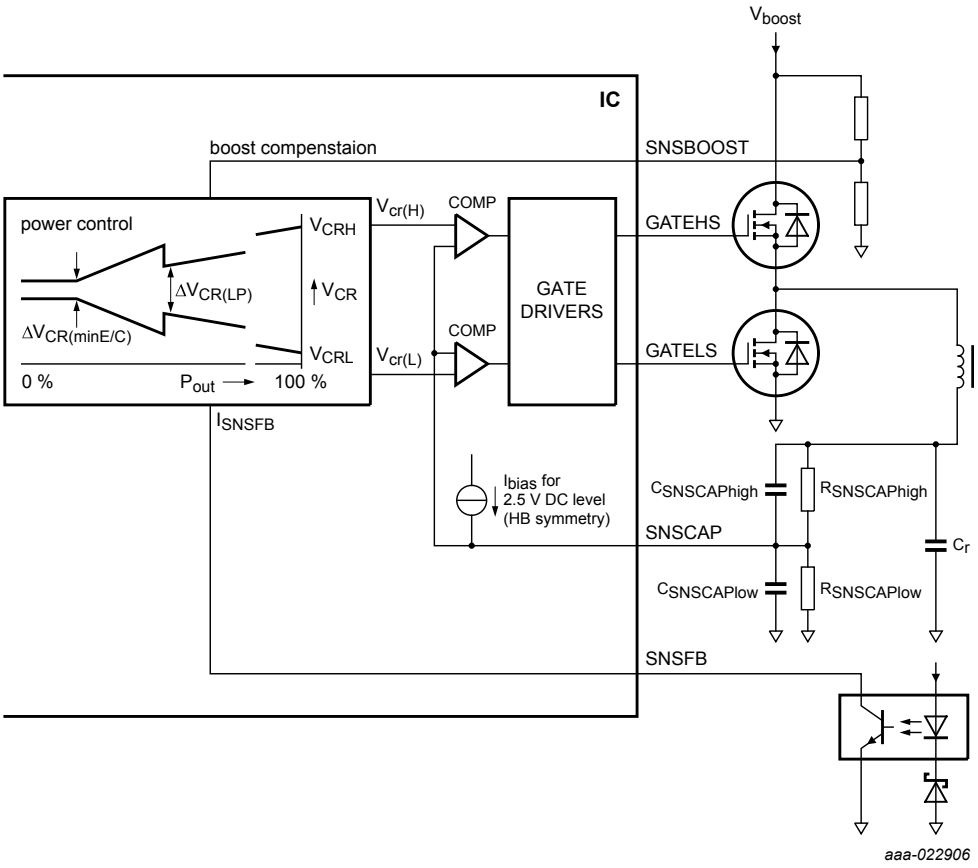


Figure 40. V_{CAP} power control and SNSCAP sensing by the capacitive divider

The SNSCAP divider scales the voltage range on Cr down to the voltage range of the TEA2016. The capacitors make the divider and the resistors contribute to the DC information to SNSCAP.

The voltage on Cr is depending on the output power and can be calculated:

$$\Delta V_{Cr\_ideal} = \frac{P_{out}}{V_{boost} \times C_r \times f_{HB}} \quad (6)$$

Because of a time delay between detecting a target power level and really switching polarity for the next half cycle, the voltage on Cr will be a bit larger than in the basic calculation. See Section 9.9.1 for a description of this delay. The difference can be calculated with the primary magnetization current when assuming the system is switching near the transition of DCM-CCM.

$$\Delta V_{Cr\_delay} = \frac{I_{mag,peak} \times \Delta t_{delay}}{C_r} \quad (7)$$

For estimating the SNSCAP divider, a certain power level must be calculated with:

$$\Delta V_{Cr} = \Delta V_{Cr\_ideal} - \Delta V_{Cr\_delay} \quad (8)$$

ΔV_{Cr} must match with the correct ΔV_{SNSCAP}.

For the 100 % power level at nominal $V_{SNSBOOST}$ (2.5 V), the ΔV_{SNSCAP} can be calculated with the formulas in Section 9.2.2.

$$\Delta V_{SNSCAP} = 2 \times \frac{1.6\ V}{2.5\ V} \times 0.0075 \times 100 = 0.96\ V \quad (9)$$

The SNSCAP divider must match the 100 % power ΔV_{Cr} with the ΔV_{SNSCAP} = 0.96 V.

Example for ΔV_{Cr}:

$$\Delta V_{Cr} = \Delta V_{Cr\_ideal} - \Delta V_{Cr\_delay} = \frac{240\ W}{390\ V \times 47\ nF \times 70\ kHz} - \frac{13\ A \times 450\ ns}{47\ nF} = 185\ V \quad (10)$$

According to this ratio, the $C_{SNSCAPlow}$ value must be greater than $C_{SNSCAPhigh}$:

$$C_{SNSCAPlow} = \frac{\Delta V_{Cr} - \Delta V_{SNSCAP}}{\Delta V_{SNSCAP}} \times C_{SNSCAPhigh} = \frac{185\ V - 0.96\ V}{0.96\ V} \times C_{SNSCAPhigh} = 192 \times C_{SNSCAPhigh} \quad (11)$$

9.2.4 Practical restrictions for SNSCAP divider

For correct functioning of the SNSCAP features, there are a few practical restrictions to design the SNSCAP divider.

- Because the internal SNSCAP 2.5 V bias source can only source current, the divider must not cause the voltage on SNSCAP to exceed the DC-level of 2.5 V. The resistive divider ($R_{SNSCAPlow}$ and $R_{SNSCAPhigh}$) part must ensure that the voltage on SNSCAP does not exceed the DC-level of 2.5 V.
- For correct operation of the bias source of SNSCAP, the value of the resistor $R_{SNSCAPlow}$ between the SNSCAP and GND must exceed 15 kΩ.
- The resistive part of the divider provides constant losses during operation and burst mode operation. To limit power losses, the total impedance should be high. For example, $R_{SNSCAPlow}$ + $R_{SNSCAPhigh}$ = 5 MΩ.

After implementing the estimated values, it is important to check the result to the power limit reference level in the real application. The power level for triggering power limit must be correct. If it is not, the divider values must be corrected (see Section 12.1.3).

When the SNSCAP divider is correct, the mode transition levels can be modified using settings.

9.2.5 SNSFB regulation

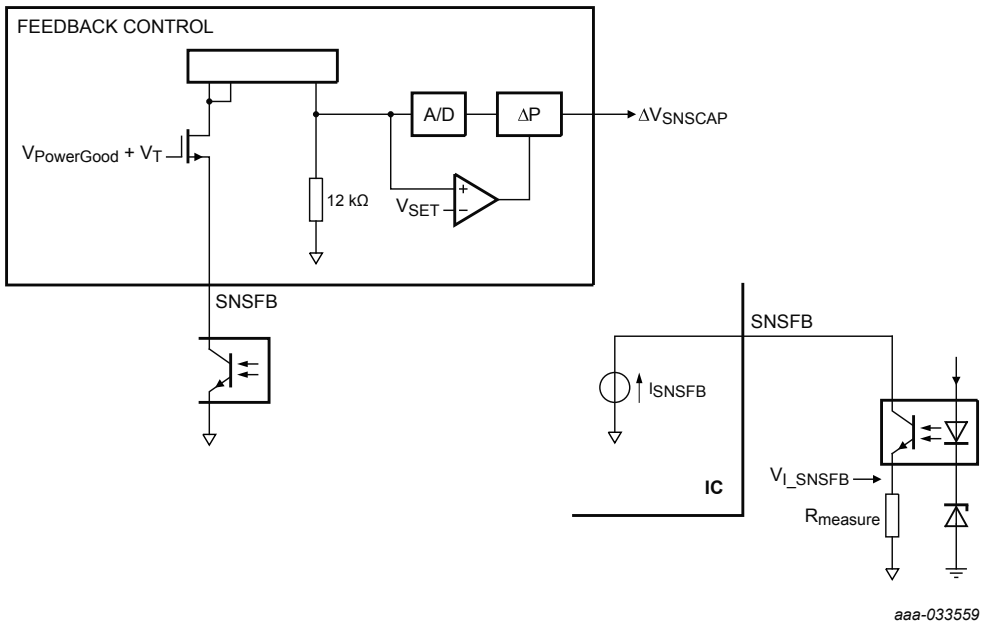
In the TEA2016AAT, a special circuit is used to always have a low current flowing in the feedback circuit. It helps to reach very low power consumption of the converter at no load or at low load conditions.

An internal bias regulation slowly regulates the average current level in SNSFB during LP and HP mode (80 µA to 1200 µA). During burst mode, the current varies but remains close to the burst start level of 20 % higher than the selected level for LP and HP.

The voltage on SNSFB or current in SNSFB do not directly show the power level of the converter. A method to monitor the regulation is to measure the current in SNSFB by adding a measurement resistor for engineering purpose.

The voltage across the measurement resistor shows the regulation at transients or changes. When running at a constant power level, the SNSFB current level is always at (for example) 80 µA in LP and HP mode. Because BM operation is based on periods of switching and not switching, there are continuously transients. Therefore in BM the SNSBF current varies according to the output regulation with a burst start level at (for example) 100 µA.

See Figure 38, Figure 45, and Figure 46 for examples on the SNSFB current behavior.



For engineering work. a series resistor can be added to observe the SNSFB current behavior. 100 Ω is a typical value for $R_{measure}$. Some care is necessary to ensure that the measurement setup does not introduce disturbances.

Figure 41. Feedback control and measurement resistor to measure the regulation current

9.3 Operation modes

To reach a high efficiency at all power levels, the TEA2016AAT uses the low-power mode (LP). This mode operates in the power region between continuous high-power mode (HP) switching and burst mode operation (BM).

The LP mode itself controls the power by energy-per-cycle control similar to the HP mode. In total, the normal output power range is split in three operation modes:

- HP mode (traditional continuous switching)
- LP mode with energy-per-cycle control
- Burst mode

To optimize the modes for application requirements, presetting can modify several parameters. Figure 42 shows an overview of the modes and modifications that can be made using settings.

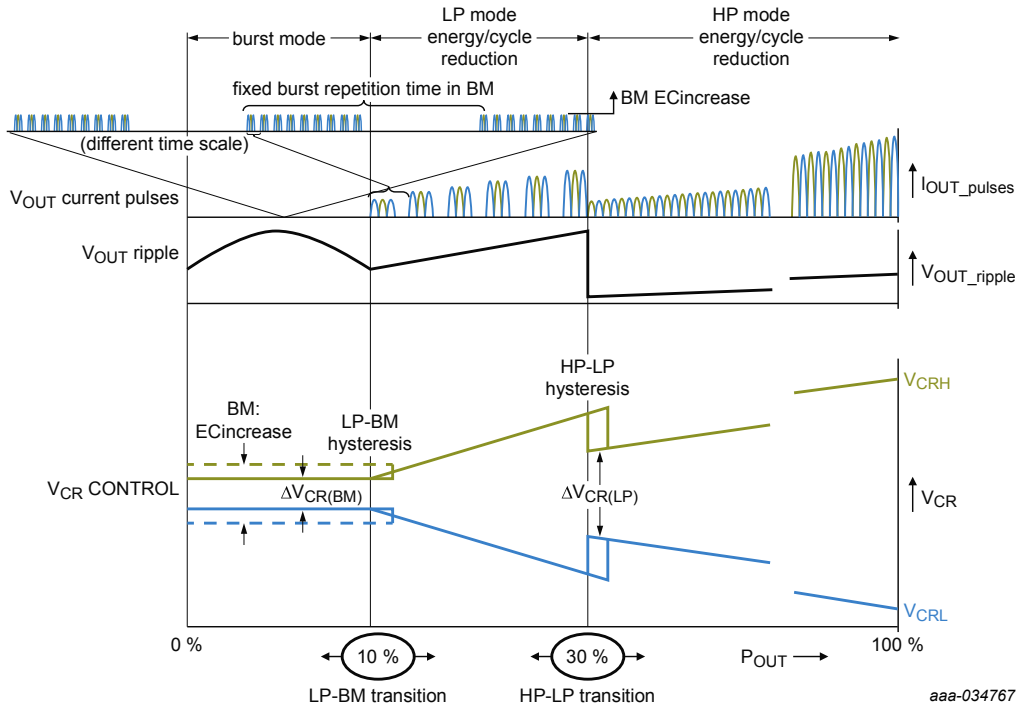


Figure 42. Operation modes and levels that can be modified using settings

9.4 HP mode

The HP mode operates in continuous 50 % duty cycle switching of the LLC. It is similar to the traditional LLC operation control by frequency. The TEA2016AAT, however, obtains the result by V_{cap} control driving for voltage levels on the resonant capacitor instead of switching by time/frequency.

In all operation modes, the V_{cap} level determines the moment when the gate drive is switched off. When reaching the correct V_{cap} level for the required output power, the gate drive is switched off.

Based on the HB end-of-slope detection, the adaptive non-overlap function switches on the gate drive.

9.5 Low-power mode

The low-power mode is a kind of burst mode at high repetition frequency. In this mode, to provide a better conversion efficiency, the energy in each pulse is kept relatively high. During the period of not switching, the losses are low. The number of peaks can set the repetition frequency of the complete LP cycle. A higher number of peaks can provide better efficiency. However, to prevent the risk of audible noise, the repetition frequency must not become too low. The transition from HP mode to LP mode can be set on a certain power level by presetting (10 % to 54 %).

9.5.1 LP mode switching

Each LP switching cycle consists of 1 conversion cycle and a period of no switching. To optimize transitions between switching and waiting, 4 extra events are added. These extra stages of the LP sequence minimize the losses in the converter transition from energy conversion to a period of waiting.

LP sequence:

1. 1st half of energy conversion
2. 2nd half of energy conversion
3. Energy dump prepare (also generates output power)
4. Energy dump
5. Waiting period
6. Energy restore

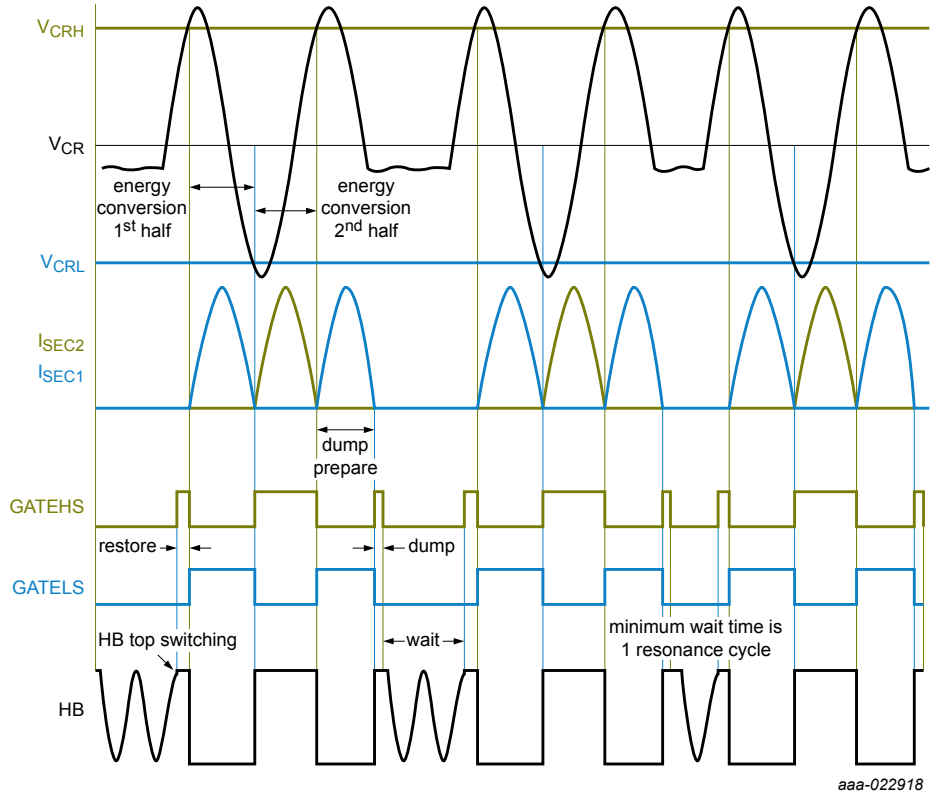


Figure 43. Low-power (LP) mode switching

9.5.1.1 The energy conversion state

This stage is like normal conversion switching. The power level is according to the required level in EC control.

9.5.1.2 Energy dump prepare

This stage is very similar to the first half of the normal energy conversion state (GATELS on). Different is the switch-off level which is earlier than normal and leads to a slightly CCM switching on the output current. This position and the dump action (GATEHS on/off) park the energy in the primary resonant capacitor on a level that minimum primary current flows after the switch-off. It reduces the losses during the waiting stage to the minimum.

9.5.1.3 Energy dump

The energy dump prepare and the energy dump park the energy in the primary resonant capacitor on a level that minimum primary current flows after switch-off. It reduces the losses during the waiting stage to the minimum. The energy dump consists of switching on/switching off GATEHS for a short time. To obtain the best efficiency or minimum output current between the 3 main current pulses, the SNSCAP level for the energy dump can be optimized using a setting.

9.5.1.4 Waiting period

The waiting period is the period of no switching where energy losses are minimal. This stage reduces the average magnetization losses, because it does not generate losses during the period of waiting.

To minimize switching losses at the end of a waiting period, the restore stage starts when the voltage on the HB node is at the maximum (top switching). The duration of the waiting period depends on the resonance behavior of the LLC. The minimum time of a waiting period is 1 resonance cycle. The LP number of peaks can extend the duration of the LP cycle by waiting a number of resonance cycles.

A longer waiting time can increase the efficiency. However, it can also increase the output voltage ripple. To avoid audible noise below 20 kHz, ensure that the LP repetition time does not become too low.

9.5.1.5 Restore

To start energy conversion after a waiting period, the resonant capacitor must be charged again to the correct V_{CAP} level. A shorter GATEHS switch-on/off action achieves the charging again to the correct V_{CAP} level. Top switching on the GATEHS shows hard switching of the HB.

9.5.1.6 Hard switching in LP

Two switching events include hard switching.

- Start of the restore by top switching
- End of the dump prepare by output CCM switching

To optimize the switching for the start restore state, the TEA2016AAT uses top switching. To prevent some extra losses or voltage overshoot, the CCM switching requires some application attention on the secondary switch (diode or SR).

The LLC burst mode also consists of LP cycles. After a burst, the HB ringing becomes almost zero. Starting a next burst shows an initial hard switching event without the benefit from top switching.

9.5.2 LP mode with energy-per-cycle control

In LP mode, the energy control mechanism is to change the power level in the energy converting stages: amplitude of the 3 current pulses to the output. V_{CAP} control driven by the SNSFB changes the amplitude.

9.5.3 LP mode repetition frequency selection

The repetition frequency of the low-power (LP) mode cycles can be selected using the number of peaks parameter. The selection options are from 1 to 8 in steps of 1. Figure 44 shows the situation for the value 2 and 4.

The ringing frequency of the HB node depends on the capacitance on the HB node and the inductance value of the LLC. The values depend on the converter design choices. The values are specific for each application.

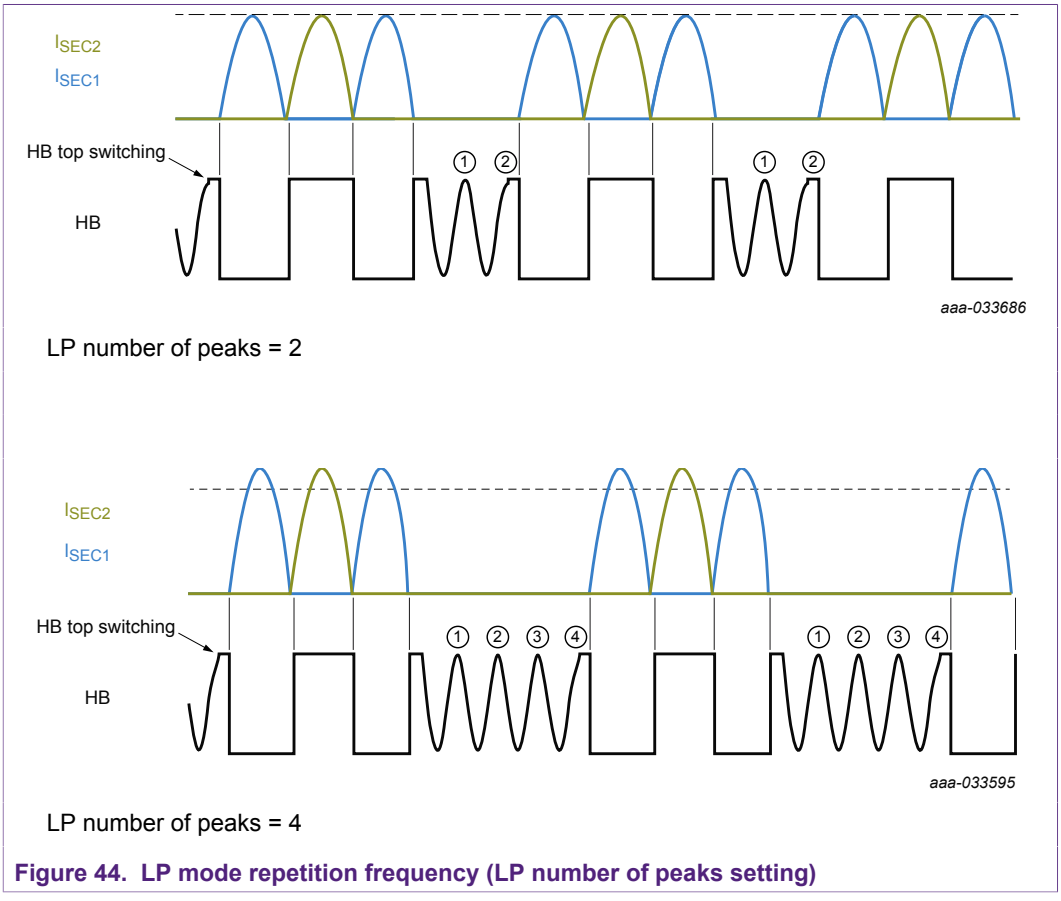


Figure 44. LP mode repetition frequency (LP number of peaks setting)

See Section 13.4.2 for additional information.

9.6 BM operation

In burst mode, each burst consists of a series of LP cycles. The burst is a period of LP switching. Each LP cycle in the burst contains the energy that is determined by presetting the minimum energy-per-cycle (EC_{min}). It corresponds with the LP-BM transition, multiplied by a factor that can be selected (1x to 8x). The number of peak settings fix the wait time of the LP cycle.

The BM fixed repetition frequency can be selected: 20 Hz to 3200 Hz.

To control the average output power, the number of LP cycles in a burst is variable. An internal algorithm that targets the fixed repetition frequency for a burst determines the required number of LP cycles in the burst.

Extending the wait time of the last LP cycle obtains the time of not switching.

A value for the minimum cycles in a burst can be selected from 1 to 12. When this minimum value is reached and the power must be reduced further, extending the period of not switching reduces the repetition frequency. The BM repetition frequency has now become lower than the preset value.

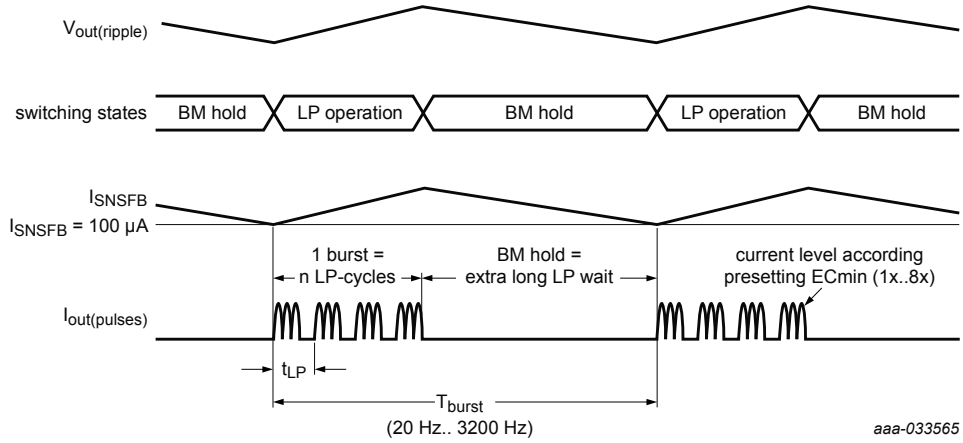


Figure 45. The burst mode system consists of LP switching and BM hold time

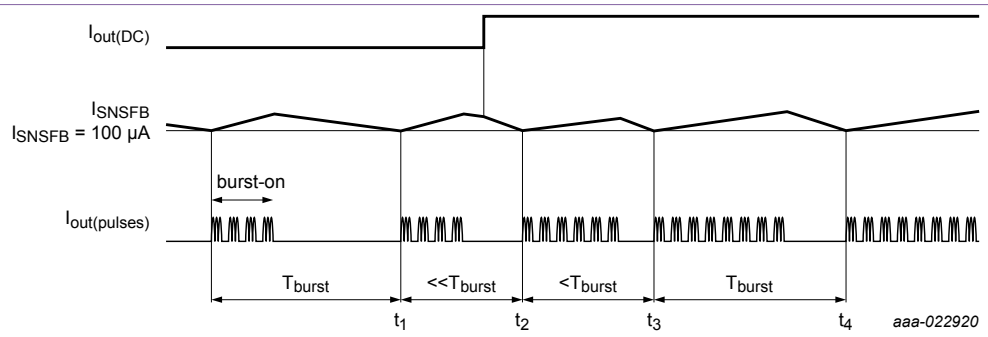


Figure 46. Regulating the number of LP cycles in a burst to adapt to a new output load for the same Tburst

9.7 Operation mode transitions

The mode transitions levels between the operating modes HP, LP, and BM can be set independently using parameters.

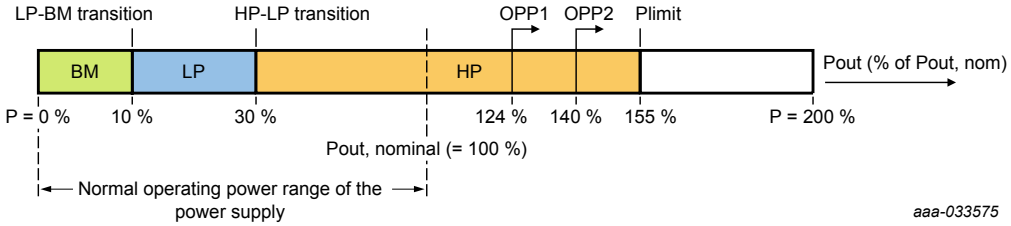


Figure 47. Mode transitions on power scale

To ensure that the selectable values match reality, the external SNSCAP divider must be designed to match the corresponding IC voltage levels. Two internal functions with selectable parameter values can be used to compensate unavoidable and application depending on time delay and offset deviations:

- dVcap offset
- zero power slope (ZPS; see Section 12.1.4)

9.7.1 HP-LP transition

The presetting of the HP-LP transition is done by a parameter between 10 % to 54 %.

At the HP-LP transition point, the energy per cycle in LP mode is compensated (larger) for the same average power level in HP mode. It provides a smooth regulation transition between the modes.

A parameter for the hysteresis: 10 % to 40 % defines the LP-HP transition. It is a percentage of the HP-LP transition value.

Example:

HP-LP = 30 %

HP-LP hysteresis = 10 %

LP-HP transition level is at 30 % + (10 % x 30 %) =33 % of the nominal power.

9.7.2 LP-BM transition

The basic presetting of the LP-BM transition is done by a parameter between 1 % to 25 %. In the default BM configuration, the level of entering and leaving BM operation is the same. When the extra long waiting time in the last LP cycle has become zero by increasing the output power, the system has left BM operation and continues in LP mode by regulating the energy per cycle.

The TEA2016AAT offers a few options to enhance BM for additional performance or requirements. The result is a less smooth transition

BM energy-per-cycle increase

Because the TEA2016AAT regulates the output via the primary capacitor voltage, it offers the ability to increase the output power per switching cycle easily when it enters burst mode. It increases the efficiency and result in a lower repetition frequency at the

lowest power levels that can help to reduce audible noise. But the output voltage ripple increases.

For the increase of output power per switching cycle, energy-per-cycle, a multiplication factor can be selected: 1 to 8. When, for instance, the factor is set to 4 and the output power slowly decreases, the system enters burst mode with an immediate “jump” to a duty cycle of 25 %.

BM-LP hysteresis

The hysteresis function is active when the energy per cycle increase is set on value higher than 1. When the system operates in burst mode and output power increases to exceed the LP- BM transition level plus a hysteresis level, the system enters low-power mode. For the hysteresis level, a value from 25 % to 100 % can be selected. It adds a percentage of the selected LP-BM transition percentage level.

Example:

If the rated output power at 100 % is 100 W, the LP-BM transition is set at 10 %, and the hysteresis is set at 50 %, the system switches from burst mode to low-power mode at a 10 % + (50 % x 10 %) = 15 % which corresponds to 15 W output power.

BM-LP hysteresis filter

To ensure a smooth transition when leaving burst mode and entering low-power mode, a burst-mode-to-low-power-mode transition filter can be set: 2 to 16 cycles. When the output power exceeds the BM-LP transition level plus hysteresis for the selected number of burst cycles, it leaves the burst mode and enters the low-power mode.

Delayed LP-BM transition

To avoid that the system jumps between burst mode and low-power mode due to small or short transient at the output, which can also cause audible noise, a delay can be set before the system enters burst mode. This time delay can be set between 0 s to 4 s. During this delay, the system keeps running in LP mode while reducing the energy per cycle to match the required output power down to zero.

To avoid too much output voltage overshoot if there is a load step from high load to low load in combination with the LP-BM delay function, a limitation is in place. If the SNSFB current shows a large overshoot, the system stops switching anyway. This SNSFB burst mode stop current ($I_{stop(burst)}$) level is two times the burst start current.

Disable BM operation

The LP-BM delay time can also be set to infinite. Selecting this option disables BM operation.

9.8 Accuracy of mode transitions

9.8.1 Time delay VSNSCAP to HB transition

The mode transition levels often show some deviation from the expected levels in an application. When the power scale is made correctly by the SNSCAP divider in accordance with the power supply requirements, the transition levels are given as a percentage of the nominal output power.

The level of transition depends on an internal SNSCAP target level and a time delay until the HB transition. The time delay consists of two parts:

1. Time between the moment that SNSCAP reached the target level (A) and the moment that the GATE switches off (B). This time is internally fixed: 150 ns.
2. Time between the moment that the GATE switches off (B) and the moment that HB reached half of its maximum value (C). This time is depending on the application properties. In this document, we assume it is 300 ns.

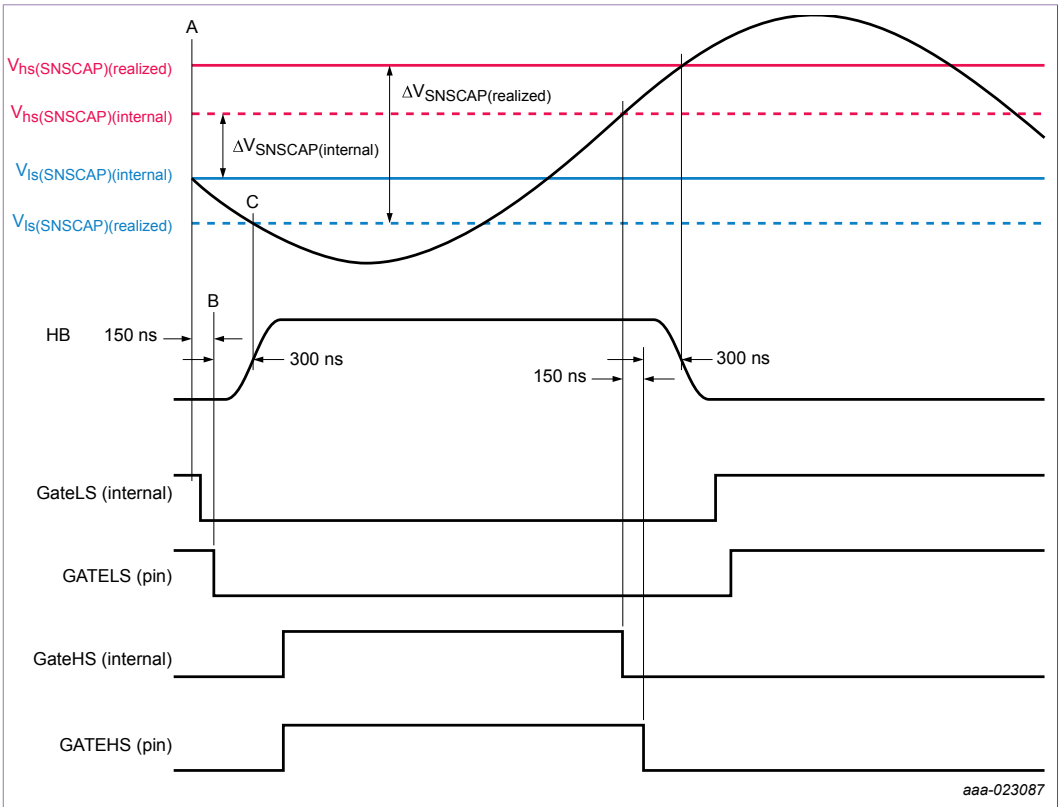


Figure 48. A time delay leads to a difference between internal and external power level

The time delay leads to a difference in power level between the control and reality, which can lead to a substantial difference in (mode transition) power levels. When the application-depending delay (B-C) is different from the 300 ns used in this document, the estimated power levels are different.

9.8.2 dVcap offset

The dVcap offset parameter can make a basic compensation for the effect of the time delay between V_{SNSCAP} and the HB transition. The best value is different for each application. When designing the values for the SNSCAP divider on V_{cap}, a practical check can be done using the dVcap function to match the power scale to the correct values. This method is discussed in Section 12.1.3 and Section 12.1.4.

9.8.3 Accuracy of mode transition levels: production spread

There are several component values and circuit properties that contribute to the resulting mode transition level. The spread at a low power level is greater than at a high power level because a constant deviation from nominal has a larger impact at lower signal levels (like the time delay discussed in Section 9.8.1.

As an example, the list of contributions for BM transition (at the lowest power level) is given in Table 4 including the specified or estimated tolerances.

Table 4. Specified and estimated tolerances of contributing functions

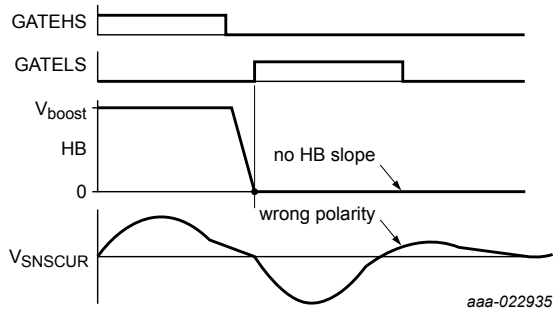
Contributing item	Tolerance (%)	Comment
resonant capacitor	5	specification
capacitive divider SNSCAP	5	specification
SNSCAP comparator levels	15	specification
time delay	6	estimation
SNSBOOST	3	estimation for boost compensation
total estimated spread	19	root of squares (valid for normal distributions)

For example, when the nominal burst mode transition level is set for 1 A output current, the transition level is between 0.8 A and 1.2 A output current in accordance with a normal distribution.

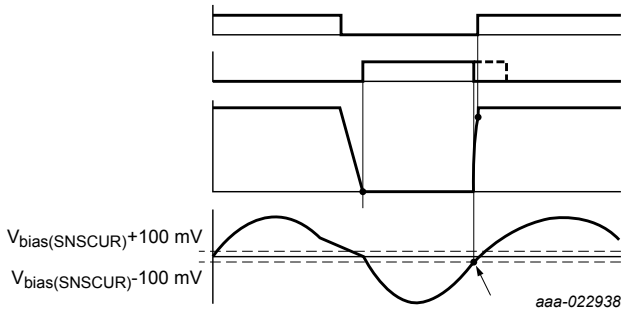
Using capacitor values with less spread can slightly improve the total tolerance.

9.9 Capacitive mode prevention by SNSCURLLC

The primary current is measured accurately, cycle-by-cycle, for the internal switching logic. Two comparators with a selectable level between 20 mV to 160 mV above and below the 2.5 V bias voltage detect when the primary current is nearing capacitive mode operation. When this level is reached before VCAP control switches off the gate, the capacitive mode prevention forces a switch-off to prevent capacitive mode switching.



a. Signals when running into capacitive mode operation



b. Capacitive mode prevention. When ±100 mV level is detected, GATEHS/GATELS is switched off.

Figure 49. Capacitive mode protection/prevention with a selected level of 100 mV

9.9.1 Practical application of CMR switching

Design choices can prevent normal capacitive mode switching. But for some applications performance parameters, like system efficiency, can only be met when allowing near capacitive mode switching in conditions where the input voltage V_{boost} drops. The CMR function in the TEA2016AAT supports it by keeping the switching inductive near the border of the capacitive mode region. The result is normally that the output power is limited and the output voltage drops.

9.9.2 Measuring SNSCURLLC

The voltage on this pin is a bit difficult to measure because attaching a probe can disturb operation. An internal bias source puts the input signal on a DC voltage level of 2.5 V. A 2.2 nF capacitor connects the AC voltage that represents the resonant current signal to this pin. The AC voltage part can best be checked on the measurement resistor R_m.

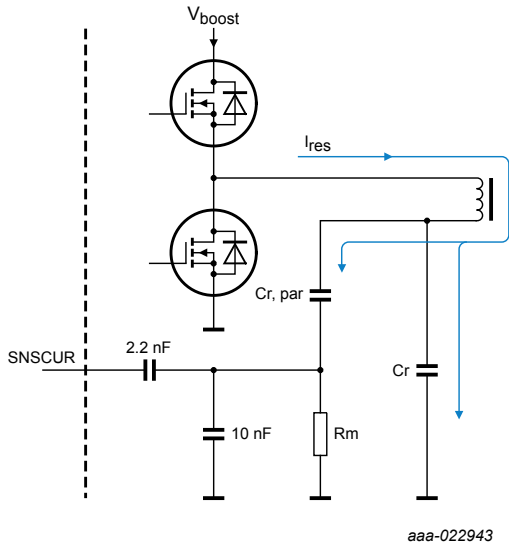
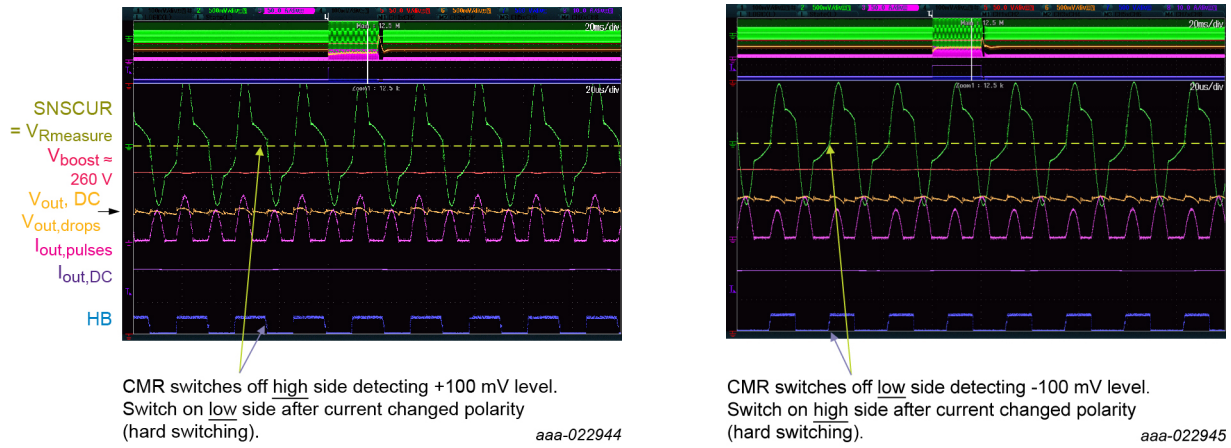


Figure 50. Typical current sensing circuit for SNSCURLLC

9.9.3 Example of CMR switching in a test condition

To observe the switching behavior during CMR, the input voltage of the LLC V_{BOOST} is supplied by a DC source of a very low operating voltage of approximately 260 V ($V_{BOOST,nom}$ = 390 V). In this condition, the converter cannot deliver more than nominal output power. When making a higher peak load, the system starts running in CMR.

The CMR switch off moment is near to the zero current level the CMR can switch off GATEHS or GATELS. Because the system regulates to 50 % duty cycle operation, it gradually changes the switching timing to achieve it. It makes the CMR changing over time.



a. Detection + 100 mV level

b. Detection − 100 mV level

Figure 51. Example of running in CMR at 100 mV during a test condition at very low V_{boost}

10 Protections

10.1 Protections overview

Table 5. Protections overview

Protection	Description	Action	PFC	LLC	Protection register
General protections					
UVP SUPIC	undervoltage protection SUPIC pins	recharge via DRAINPFC; restart when VSUPIC > $V_{start(SUPIC)}$	off	off	-
MTPfail	reading of the internal MTP failed	continue reading until the data is valid; only checked once at start-up	off	off	y
OTPint	internal overtemperature protection	LLC and PFC are either latched or safe restart	off	off	y
OTPext	external overtemperature protection	LLC and PFC are either latched or safe restart	off	off	y
SCP SNSBOOST/ FAST DISABLE	short-circuit protection/disable PFC and LLC	restart when $V_{SNSBOOST}$ > $V_{scp(start)}$	off	off	y
PFC protections					
brownout-mains	undervoltage protection mains	restart when the mains voltage exceeds the brownin level	off	on/ off[1]	-
OVP SNSBOOST	overvoltage protection boost voltage	restart when $V_{SNSBOOST}$ < $V_{ovp(SNSBOOST)}$	off	on/ off[1]	y
OVP DRAINPFC	overvoltage protection DRAINPFC voltage	LLC and PFC are either latched or safe restart protections	off	off	y
OCP	overcurrent protection	PFC MOSFET switched off; continue operation	-	-	y
PFCcoil short	-	LLC and PFC are off, followed by a safe restart	off	off	-
I_{inrush}	inrush current protection	PFC MOSFET switched off; PFC switching period extended	off	on	-

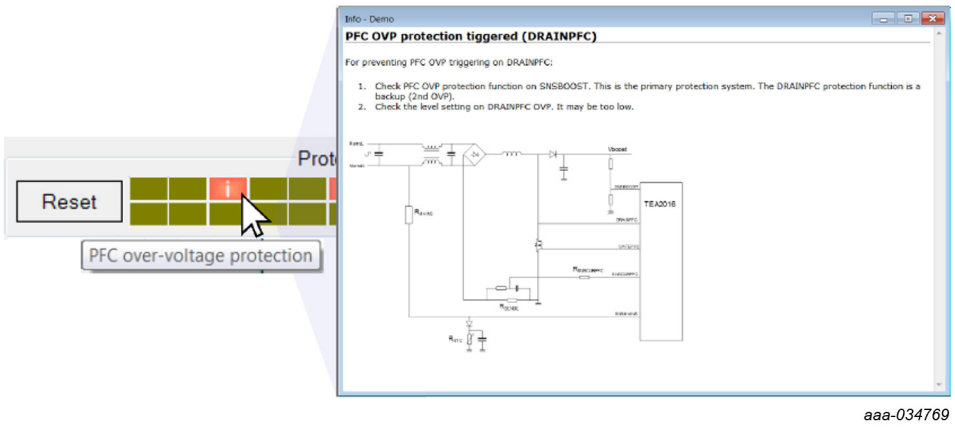
Protection	Description	Action	PFC	LLC	Protection register
LLC protection					
UVP SUPHS	undervoltage protection SUPHS pin	GATEHS = off	-	off	-
UVP SNSBOOST	undervoltage protection boost	restart when $V_{SNSBOOST} > V_{start(SNSBOOST)}$	-	off	-
OVP SUPIC	output overvoltage protection; measured via the SUPIC pin	LLC and PFC are either latched or safe restart	off	off	y
$I_{opto(max)}$	maximum optocurrent	LLC and PFC stop switching until the optocoupler current drops to below the burst level	-	-	y
On-time min	minimum on time	GATEHS or GATELS remains on	-	-	-
On-time max	maximum on time	GATEHS or GATELS turns off: continue operation	-	-	y
CMR	capacitive mode regulation	system ensures that mode of operation is inductive	-	-	y
OCP	overcurrent protection	switch off cycle-by-cycle; after several consecutive cycles, LLC and PFC are either latched or safe restart	off	-	y
$t_{startup(max)}$	maximum start-up time	LLC and PFC are either latched or safe restart	off	off	y
OPP	overpower protection	LLC and PFC are either latched or safe restart	off	off	y

[1] External components can set the latched/safe restart action.

10.2 Protection registers

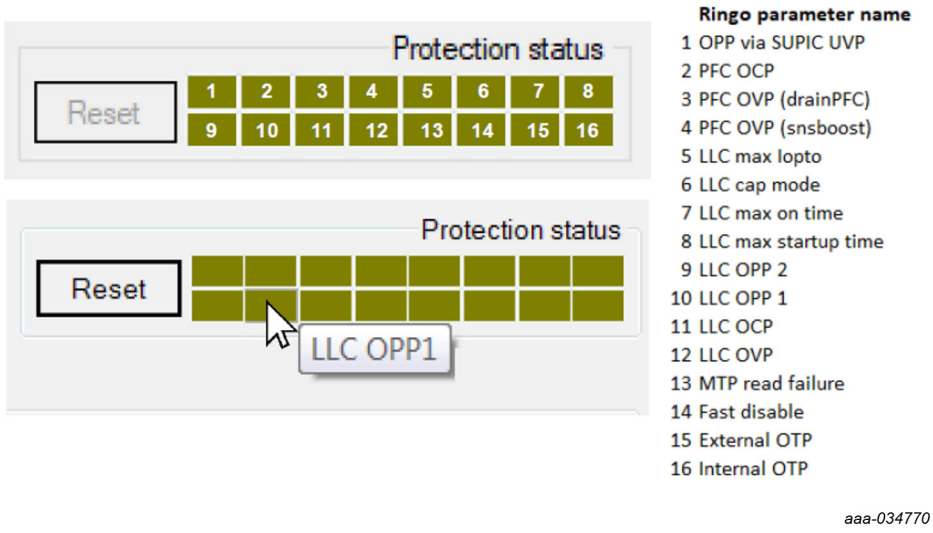
When a protection is triggered, the TEA2016AAT sets a protection bit in the MTP.

Bits of protections that are triggered are stored in the MTP. The Ringo GUI can show them as an orange color “LED”. For analysis, this information is always available, even when the MTP is read locked.



aaa-034769

Figure 52. An MTP protection register bit that was set shows orange in Ringo GUI



aaa-034770

Figure 53. MTP: 16 protection register bits

10.3 General protections

10.3.1 UVP SUPIC

When the SUPIC voltage has reached the start level of 19 V or 12 V (selectable), the IC enables operation. If supplied by the HV source, the voltage is regulated with a hysteresis of 0.7 V. When the SUPIC voltage drops to below 10 V, the UVP SUPIC protection stops operation. A system reset is activated at 9 V.

During the non-switching period in burst mode, when the SUPIC voltage drops to 12 V, the HV source is activated to avoid the system from stopping during a very long period of non-switching. The HV source regulates the SUPIC voltage with a hysteresis of 0.7 V above 10 V (see Section 6 for the SUPIC functionality).

10.3.2 MTP fail

For correct operation, the stored MTP setting values are copied to the registers at start-up.

The IC operation works with the register values. It can only store the protection registers in the MTP memory. The user or a programming unit must store the remaining MTP content.

When reading the MTP values at start-up fails, the operation cannot start. The MTP read failure bit in the protection register is set. The IC continues to try to read the MTP.

The protection registers can be checked with the GUI program.

10.3.3 Overtemperature protection (OTP)

The TEA2016AAT provides two OTP protections:

- Internal OTP
- External OTP

10.3.3.1 Internal OTP

The IC contains an internal temperature protection. When the internal temperature exceeds 135 °C, the internal OTP is triggered. It follows the same response as selected for the external OTP, being either latched, safe restart or latched after several restart trials.

10.3.3.2 External OTP

The external application temperature is measured via an NTC connected to the SNSMAINS pin. To measure the external NTC value, an internal current is used. The value of this current can be between 150 µA and 1050 µA.

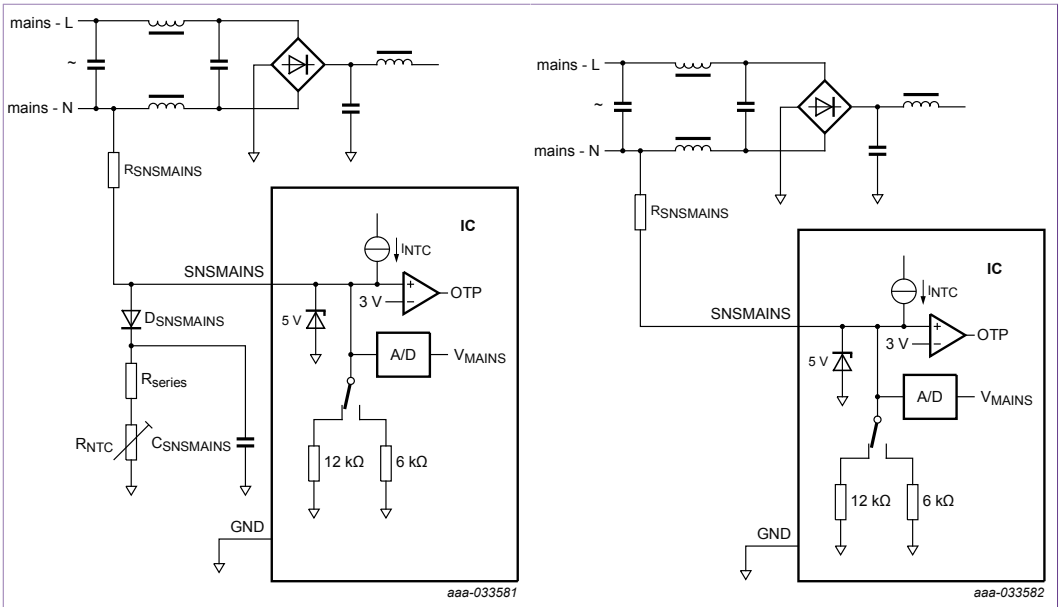
To avoid false triggering of the external OTP, a delay time can be set between from 0.5 s to 8 s. Because the NTC measurement follows the mains cycles, the OTP delay can deviate because of the mains frequency.

The follow-up of this protection can be selected. It is a safe restart protection or a latched protection. The latched protection includes an option to make a number of safe restarts before the latched protection becomes active (see Fig 82). If the latched protection must become active immediately, the value can be set to 0.

10.3.3.3 Not using the external OTP function

When no external OTP function is necessary, the external OTP components can be omitted.

To disable the external OTP function in the IC, set the current level to 0 µA.



a. SNSMAINS with external OTP

b. SNSMAINS without external OTP

Figure 54. SNSMAINS with and without OTP function via external NTC

10.3.4 SCP SNSBOOST and FAST DISABLE function

By pulling down SNSBOOST, the system operation can be stopped. The way that this function behaves is selectable:

- On/off:
  Immediately stop when SNSBOOST becomes low. And startup again when SNSBOOST is released.
- Safe restart:
  Immediately stop when SNSBOOST becomes low and follow up with safe restart until SNSBOOST is released.
- Latched:
  Immediately stop when SNSBOOST becomes low and follow up with a latched protection.

When SNSBOOST is short circuited to ground because of a fault condition, the behavior of the protection is as described above (see Section 12.5).

10.4 PFC protections

10.4.1 UVP SNSMAINS (brownout)

At a selectable current level from 4.95 µA to 13.35 µA, the brownin level is reached and the IC starts switching. When the current drops again under the selectable hysteresis relative to the brownin level (0.15 µA to 1.2 µA), the brownout level is reached and the IC switching stops.

When, during PFC operation, the current level drops to below the selected mains brownout level, an internal timer of a selectable brownout delay value from 25 ms to 1200 ms is started. The current level must remain below the brownout level during this period before the brownout protection is activated.

At brownout, the PFC operation is stopped. There is an option to stop the LLC operation after a selectable time between 125 ms to 6000 ms. When the value is set to off, the LLC remains operating (see Section 8.2).

10.4.2 OVP SNSBOOST

The PFC output voltage is measured via the SNSBOOST and DRAINPFC pins. These independent functions provide a PFC output overvoltage protection (OVP). A number of settings define the PFC OVP.

When an OVP is detected at the selected SNSBOOST pin voltage level, the PFC stops switching immediately. When the SNSBOOST voltage drops below the regulation level (2.5 V), it continues operation again. For this function, no follow-up option for the safe restart protection or latched protection is available.

The SNSBOOST PFC OVP level can be selected between 2.6 V and 2.7 V.

10.4.3 OCP SNSCURPFC

The maximum PFC peak current is limited cycle-by-cycle through sensing the voltage across an external sense resistor in series with the mains bridge rectifier. The result is a negative voltage measured on the SNSCURPFC pin. It is limited to −300 mV. When the SNSCUR voltage reaches −300 mV, the MOSFET is switched off (see Section 8.17).

10.4.4 PFC coil short

The SNSCURPFC OCP limitation function provides a protection for a PFC coil short circuit condition. At each GATEPFC switch-on event, the system switches off immediately at the −300 mV OCP level. When it continues during 100 ms, the PFC OCP protection is activated followed by a safe restart. A PFC OCP protection sets a protection register bit.

10.4.4.1 Inrush current limiting

The SNSCURPFC OCP limitation function provides a protection during inrush or mains-surge events. At each GATEPFC switch-on event, the system switches off immediately because of reaching the −300 mV OCP level. It limits the current in the PFC MOSFET.

If this condition continues during 100 ms, the PFC OCP protection is activated followed by a safe restart. The time counter for the 100 ms protection function works with an up/down counter mechanism that subtracts time when a PFC cycle does not trigger the OCP level.

A PFC OCP protection sets a protection register bit.

10.5 LLC protections

10.5.1 UVP SUPHS

When the voltage across C_{SUPHS} (= V_{SUPHS} – V_{HB}) drops below 7 V, the driver stops operation to prevent unreliable switching (see Section 6.5).

10.5.2 UVP SNSBOOST

When the voltage at the SNSBOOST drops to below a selectable LLC brownout level (1 V to 2.05 V), the LLC converter enters the protection state. When the SNSBOOST voltage exceeds the start level (LLC brownin) again, the LLC converter starts switching again (see Section 9.1).

10.5.3 Overvoltage protection (OVP) on SUPIC

In a resonant converter, the voltage at the SUPIC pin reflects the output voltage. When the SUPIC voltage exceeds a defined level, the OVP protection is triggered. The level can be set from 1 V to 15 V above the selected start level in steps of 1 V.

To avoid false triggering, a delay can be set from 10 µs to 800 µs. The response of this protection can be latched, safe restart, or latched after several restart trials. Setting the delay to infinite disables this OVP function.

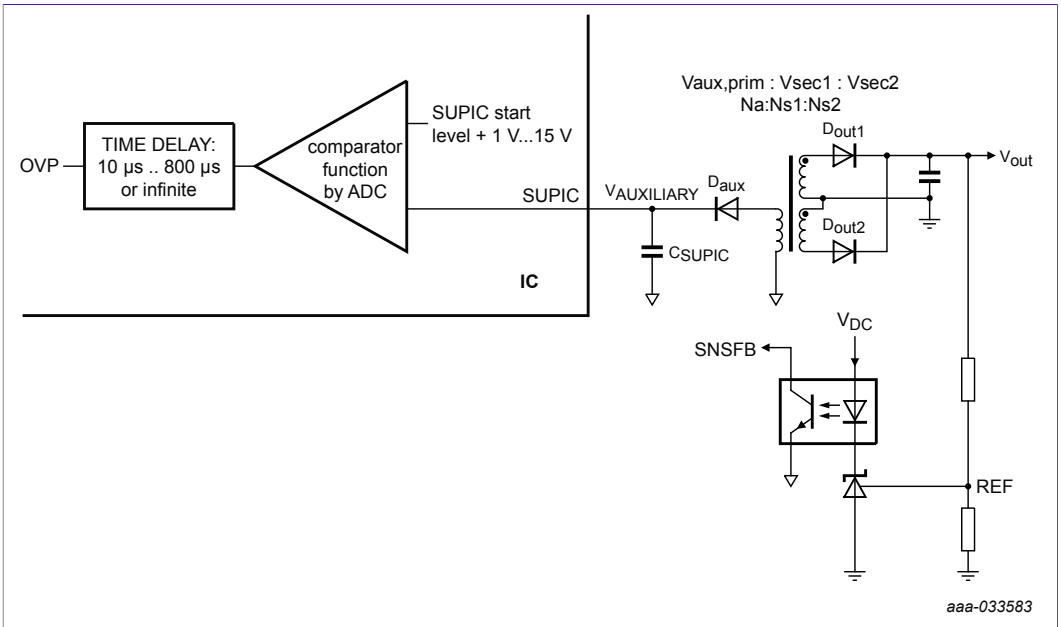


Figure 55. Overvoltage protection (OVP) on SUPIC

10.5.3.1 Auxiliary winding construction for OVP sensing

When dealing with a mains insulated converter, the LLC output voltage can be measured using the auxiliary winding of the resonant transformer. To measure the secondary voltage of the primary circuit auxiliary winding accurately, a special transformer construction is required.

For the winding to work correctly, it must have a good coupling with the secondary winding and a minimum coupling with the primary winding. So, a good representation of the output voltage situation is obtained (see Section 6.3.2).

To meet the mains insulation requirements, triple-insulated wire can be used.

10.5.3.2 Calculation of OVP sensing by auxiliary winding

This section provides a method that can be used to estimate the accuracy of indirect output voltage sensing by using an auxiliary winding (see Figure 55 for names and functions).

Transformer ratio:

- Na = number of turns on auxiliary winding
- Ns1 = number of turns on secondary (output) winding 1
- Ns2 = number of turns on secondary (output) winding 2
- Ns1 = Ns2 = Ns

$$V_{auxiliary} = V_{out} \times Ns \;/\; Na \tag{12}$$

Voltage drop over the rectifier diodes:

- D_{AUX} = voltage drop over the diode of the auxiliary voltage
- D_{OUT1} = voltage drop over the diode1 of the output voltage
- D_{OUT2} = voltage drop over the diode2 of the output voltage

$$D_{OUT1} = D_{OUT2} = D_{OUT} \tag{13}$$

Combining (a) + (b):

$$V_{auxiliary} = \left(\left(V_{out} + D_{out}\right) \times Ns \;/\; Na\right) - D_{AUX} \tag{14}$$

10.5.3.3 Differences between theory and practice: calibration

Because of several reasons (some of them given in the remarks), the calculated value can deviate from the practical value. Still, the formulas provide the relationships between several parameters.

If a parameter in practice deviates from the theoretical nominal (for example +5 %), it can be used to “calibrate” the theoretical calculation to the reality.

If there is a significant contribution, tolerance analyses can be done using the calibrated calculation.

10.5.3.4 Example of calibration and an estimation of tolerance

$$V_{SUPIC\_OVP} = \left(\left(V_{out} + D_{out}\right) \times Ns / Na\right) - D_{AUX} \quad (15)$$

Examples:

$$V_{SUPIC\_OVP} = \left(\left(V_{out} + 0.7\ V\right) \times 3 / 2\right) - 0.7\ V$$

$$V_{out} = \left(\left(23 + 0.7\right) \times 0.667 - 0.7\right)\ V = 15.1\ V = V_{OUT\_OVP\_CALCULATED} \quad (16)$$

Calibration by using OVP measurement results from the real application:

I_{out} = 0.1 A: V_{OUT_OVP} = 15.2 $V_{(measured)}$
I_{out} = 10 A: V_{OUT_OVP} = 15.1 $V_{(measured)}$
I_{out} = 20 A: V_{OUT_OVP} = 15.0 $V_{(measured)}$

Correction:

$$V_{OVP\_REALITY} = V_{OUT\_OVP\_CALCULATED} - 0.01\ I_{out} + 0.1\ V$$

OVP protection tolerance analyses:

Analysis for the worse case condition when I_{out} = 0.1 A and the measured level for OVP was V_{OUT_OVP} = 15.2 V.

$$V_{OUT\_OVP} = \left(23 + 0.7\right) \times 0.667 - 0.7 + 0.1 = 15.2\ V\ \left(nominal\right)$$

Table 6. List of tolerances

V_{SUPIC_OVP}	6 %	(TEA2016AAT data sheet)
forward voltage diode	10 %	(estimation; assumption)
transformer ratio	3 %	(transformer specification)
calibrating factor	10 %	(estimation; assumption)

Using all worst-case tolerance (highest voltage):

$V_{OUT\_OVP} = \left(24.38 + 0.77\right) \times 0.687 - 0.63 + 0.11 = 16.75\ V\ \left(worst\ case\right)$
; 10 % higher than the nominal of 15.2 V

Using the statistical method of root of squares method for nominal distributions and neglecting the minor contributions (forward voltage + calibration factor):

$$V_{OUT\_OVP} = V_{SUPIC\_OVP} \times Ns / Na\ \left(statistical\right)$$

Expected tolerance:

$$\sqrt{\left(6^2 + 3^2\right)} = 6.7\ \%$$

10.5.3.5 Output voltage rise because of time delay

The filter for false protection triggering introduces a waiting time until protection. In fault condition, the output voltage continues to increase during this period.

The additional voltage on the output can be estimated by measuring the systems voltage rise (dV/dt) and multiply this measurement with the selected OVP delay time.

Example:

Measured at start-up with no output load, the voltage near the OVP protection level increases with 50 mV/10 µs. When the delay time is set on 50 µs to avoid false triggering by spikes, a 5 × 50 mV = 250 mV i of the output voltage can be expected.

Together with the estimated tolerance value, the maximum output voltage can be found.

Using the example from Section 10.5.3.4, the statistical tolerance was 6.7 % on a nominal setting of 15.2 V. The maximum voltage, including the output rise from these examples, is

$$15.2\ V + \left(6.7\ \% \times 15.2\ V\right) + 0.25\ V = 16.47\ V$$

.

OVP sensing on the secondary side can improve the tolerance.

10.5.3.6 OVP triggering by external signal

A latched protection or safe restart protection can be activated by pulling SNSBOOST to GND, using an optocoupler and secondary output voltage sensing.

The accuracy of the OVP sensing on the secondary side output is better than by auxiliary winding. But some extra circuit is required.

Now tolerance is only related to the measurement resistors (normally 1 % or less) and the OVP comparator (several commercial types offer 2 % or 1 % accuracy). The resulting statistical tolerance can be reduced to 2 % or less.

10.5.3.7 Disable OVP function

Setting the delay time to infinite disables the SUPIC OVP function.

10.5.4 Maximum optocurrent during burst mode

When the system operates in burst mode, it adjusts the number of LP cycles such that the burst frequency corresponds to the selected burst frequency setting value. If, during these switching cycles, the output load decreases, the output voltage increases because the system has calculated the number of required switching cycles based on a previous situation.

If the measured optocoupler current at the SNSFB pin exceeds a certain level during a load step, the system ends the burst switching cycle to prevent that the output voltage increases too much. This optocoupler maximum current protection level can be between 2.5 and 7.5 times the selected optocoupler bias current level.

10.5.5 Minimum on-time GATELS or GATEHS

To prevent that disturbance (by HB slope) triggers a switch-off of GATELS or GATEHS too early, the minimum switch on-time duration is 1.2 µs.

10.5.6 Maximum on-time GATELS or GATEHS

When the on-time of the GATELS or GATEHS exceeds the maximum on-time, the switch is turned off and the LLC converter starts the next cycle. This timeout setting can be selected between 10 µs and 40 µs. This protection sets the minimum LLC switching frequency.

10.5.7 Capacitive mode regulation (CMR)

A forced switch-off at 2.5 V plus a selectable level between ±20 mV and ±160 mV on SNSCURLLC implements the capacitive mode regulation (see Section 9.9.3).

10.5.8 Overcurrent protection (OCP) on SNSCURLLC

A small capacitor parallel to the resonant capacitor can sense the resonant current. A resistor R_m in series with this parallel capacitor shows a voltage that corresponds with the amplitude of the resonant current. This voltage can be used as input for the SNSCURLLC.

A 2.2 nF capacitor must connect the measured voltage to SNSCURLLC. The internal SNSCURLLC circuit adds a 2.5 V voltage bias to the signal on the pin.

SNSCURLLC provides three functions:

- If SNSCURLLC exceeds 2.5 V ±1.5 V, the gate driver is switched off to limit the power to the OCP level. After a selectable number of triggered cycles, a protection is activated.
- If SNSCURLLC-VBIAS 2.5 V ± a selectable low voltage level for detecting the (almost) zero current level. The driver switches off to prevent capacitive mode switching.
- SNSCURLLC-VBIAS 2.5 V ±13 mV for detecting the current polarity. It is used as parameter in the internal switching logic.

If the measured voltage on R_m exceeds the overcurrent level of ± 1.5 V (4 V or 1 V on SNSCURLLC), the corresponding switch (GATELS/GATEHS) is turned off, but the system continuous switching. In this way, the primary current is limited to the OCP level. If the OCP level is exceeded for a selectable number of consecutive cycles (GATELS and/or GATEHS), the system stops switching and enters the protection mode.

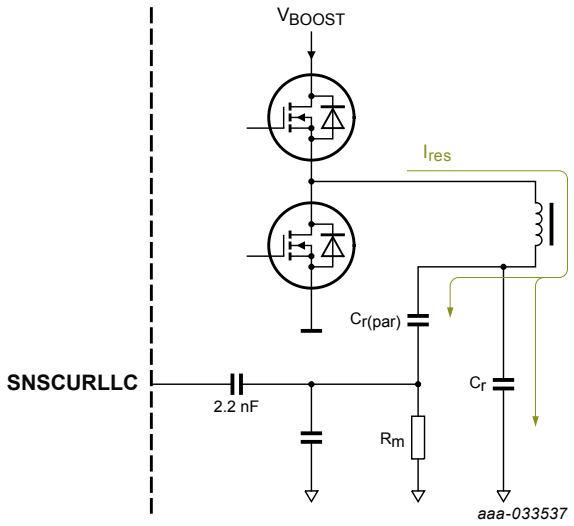


Figure 56. Typical current sensing circuit for SNSCURLLC

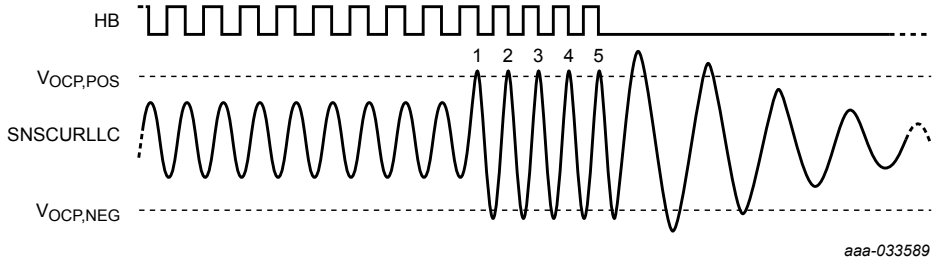


Figure 57. OCP protection stops operation after the default setting value of 5 triggers

If the current measurement circuit in Figure 56 is used:

$$V_{SNSCUR,peak} = R_m \times \left(\frac{C_{r(par)}}{C_{r(par)} + C_r}\right) \times I_{res,peak} \quad (17)$$

The transformer (effective) turn ratio defines the relationship between the primary converter current and the secondary converter current.

$$I_{res,peak} = \frac{N_s}{N_p} \times I_{out,peak} \quad (18)$$

In practice, the effective ratio between the currents is lower than the theoretical ratio of N_s/N_p. A measurement shows the correct value for a specific design. The relationship between the peak output current and the DC output current depends on the shape of the peak current. In practice, the multiplication factor (MF) is determined for a specific design near the protection level. Normally, a value close to 2.

$$I_{res,peak} = MF_{peak\text{-}to\text{-}DC} \times I_{out,DC} \quad (19)$$

When combining the various equations, the total relationship becomes:

$$V_{SNSCUR,peak} = R_m \times \frac{N_s}{N_p} \times MF_{peak\text{-}to\text{-}DC} \times I_{out,DC} \quad (20)$$

It is not possible to measure the voltage levels on SNSCURLLC during operation because a voltage probe introduces serious disturbance. To monitor the behavior, check the signal across R_m.

10.5.9 Disabling the overcurrent protection (OCP)

Selecting the filter option for "infinite" can disable the OCP protection function. The current limitation function of the OCP remains active but the system does not stop switching because of OCP triggering.

10.5.10 Maximum start-up time

When the LLC converter starts switching, it expects that the output voltage reaches its regulation level (SNSFB optocurrent) within a maximum start-up time. The maximum start-up time can be selected between 25 ms and 200 ms.

10.5.11 Overpower protection (OPP)

To prevent component overstress like excessive heating, the output power is limited by the overpower protection (OPP) function. It allows a short period of higher power before the protection is activated. An absolute maximum output power can be set using the power limit function (see Section 12.7 and Section 16.13.10).

The TEA2016AAT offers the possibility to define two independent overpower protection (OPP) functions. Most systems only require one OPP function. For protection, OPP time 2 can be set to infinite.

The definition of the OPP function consists of two setting values:

- Power level at which the protection timer is activated (Start OPP timer level): 0 % to 50 %.
- Time until the protection is activated and the system stops operation (OPP time to protect): 50 ms to 3000 ms.

The OPP power level is defined relative to the power limit setting.

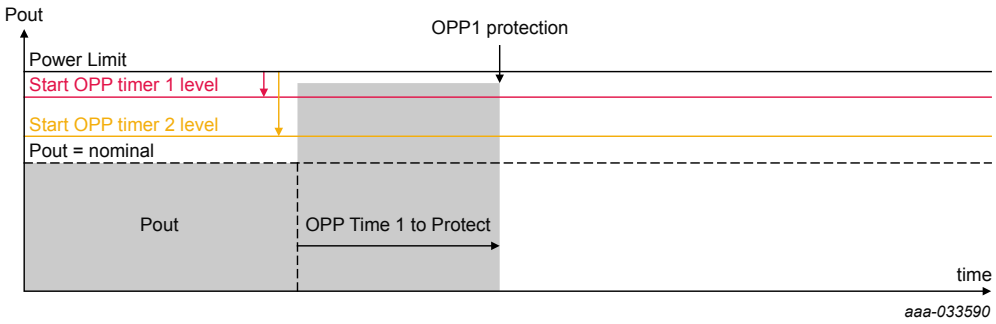
For example:

If the power limit setting is 170 % and the start OPP timer 1 level is set on −20 %, the OPP timer 1 starts at 170 % − (0.2 × 170)% = 136 % power level.

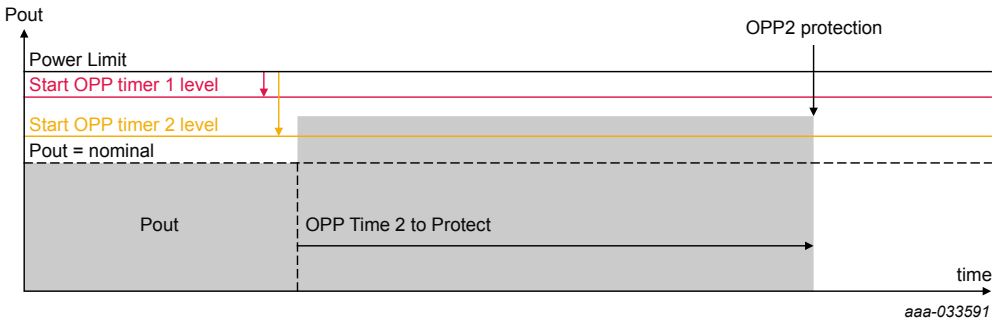
2 OPP functions: OPP1 and OPP2

In a system with two OPP functions, OPP1 is chosen at a higher power level with a shorter time to protection. OPP2 is chosen at a lower power level allowing a longer time to protection.

Both OPP functions are independent and can be set according to the system requirements.



a. OPP1



b. OPP2

Figure 58. Example of a typical choice for 2 different OPP protection levels and and 2 different times to protection

Selecting an infinite time to protect, disables the OPP functions.

10.6 Up/down counter systems

Several protection functions have a delay before protection by counting the number of triggers. When the protection level is borderline, some cycles trigger the protection level and some not. For handling this situation, an up/down counter system is used

There are two types of up/down counters used

- Fixed up/down counter: 1 up and 1 down.
- Selectable up/down counter: 1 up and a selectable value for down count 1, 2, 4, or 8.

If the down count value is 2, it means that to reach the same counter value again, two events must exceed the level for each event that does not exceed the protection levels.

Table 7. Overview of up/down counters for protection

Protection name	Number of counts up	Number of counts down
OPP1	1	1, 2, 4, or 8
OPP2	1	1, 2, 4, or 8
LLC OCP (positive level)	1	1
LLC OCP (negative level)	1	1

Protection name	Number of counts up	Number of counts down
PFC OCP	1	1
SUPIC OVP	1	1, 2, 4, or 8
DRAINPFC OVP	1	1
SNSBOOST OVP (to stop PFC)	1	1
External OTP	1	1

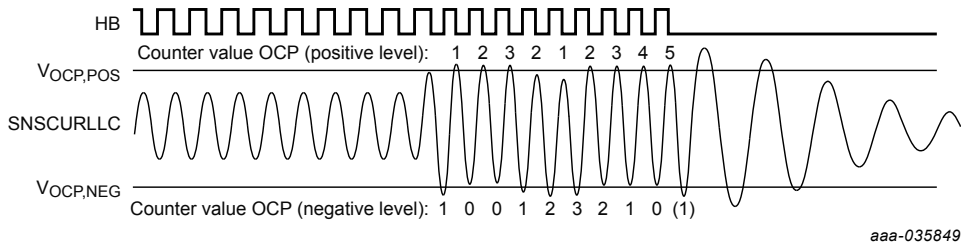


Figure 59. Example of up/down counter on LLC OCP (protection filter = 5 cycles)

11 Audible noise

In PFC + LLC power supplies that use burst mode operation, there is a risk of generating audible noise. In most applications, the LLC transformer is the main source for audible noise in burst mode operation.

11.1 Audible noise PFC converter

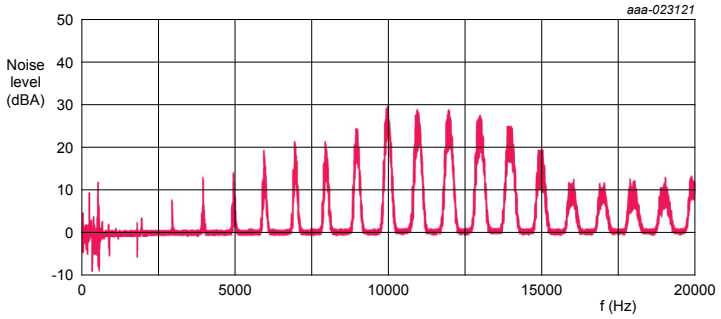
To minimize audible noise in the PFC burst mode, a presettable soft start and soft stop is included to prevent steep transients of PFC coil magnetization. The PFC burst mode operations can be set to work independently from the LLC burst mode operation. PFC burst mode SNSBOOST ripple is set for one of the options to regulate burst mode by output voltage hysteresis. However, it can also be set to synchronize with the LLC burst by selecting the ripple = off option.

At low output power, the LLC controller enables or disables PFC burst mode operation. It activates the PFC burst mode in the lower part of the LLC burst mode range based on the duty cycle of the LLC burst. Normally, when the LLC burst duty cycle is below 50 %, the PFC starts bursting. When the LLC duty cycle exceeds 75 %, it goes out of burst. When the LLC energy-per-cycle increase function is used, the behavior becomes a bit different. There is a “jump” in the LLC duty cycle and, in most cases, LLC and PFC are always in burst mode at the same time.

11.2 Audible noise LLC converter

The converted energy in LLC does not contribute to generate audible noise because the switching repetition exceeds the audible frequency. However, in burst mode, the repetition frequency of the bursts is in the audible frequency range. The TEA2016AAT can be set to a range of values for a fixed repetition frequency. This burst mode operation can generate audible noise.

The main mechanism for producing noise is the interruption of magnetization current sequences (bursts) leading to a mechanical force. The core of the resonant transformer is especially susceptible and starts acting like a loudspeaker. The noise amplitude is highest at the (mechanical) resonant frequency of the transformer. Normally, it is a higher frequency than the burst repetition frequency itself. Harmonics of the burst repetition frequency produce the audible noise.



Harmonics of 1 kHz produce most noise at the audio noise resonance frequency of the transformer. For this transformer, the resonance is around 11 kHz.

Figure 60. Example of noise spectrum with 1 kHz burst repetition frequency

Low-power mode

The LP repetition frequency must be set to keep switching above the audible frequency. The main control is the LP number of peaks setting. A higher number results in a lower LP repetition frequency.

Burst mode

The burst mode switching consists of LP cycles. Also, for audible noise in BM, the LP repetition frequency must be set to exceed the audible frequency range.

The TEA2016AAT offers 4 parameters that help to reduce audible noise for LLC burst mode operation.

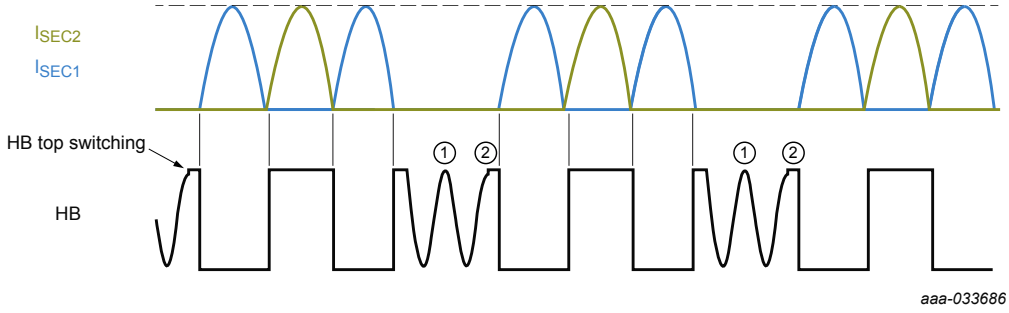
- LP number of peaks:
  A lower number of peaks increases the LP repetition frequency to above 20 kHz with margin. A value of 1, 2, or 3 usually gives a good result. However, the repetition frequency strongly depends on the HB ringing frequency of a specific application (see Figure 61).
- BM repetition frequency:
  A lower repetition frequency reduces the audible noise. Because it also increases the output voltage ripple, the output voltage requirements limit this setting (see Figure 62).
- LLC burst mode number of soft start cycles:
  The use of BM soft start reduces the audible noise of the LLC transformer. Usually, a soft start of 2 cycles (is 1 complete LP cycle) provides a good improvement. But the number of cycles can be optimized for each application by checking the resulting noise level (see Figure 63).
- LLC burst mode number of soft stop cycles:
  The use of BM soft stop reduces the audible noise of the LLC transformer. Usually, a soft stop of 2 cycles (is 1 complete LP cycle) provides a good improvement. But the number of cycles can be optimized for each application by checking the resulting noise level (see Figure 63).

Indirectly, the BM operation design also contributes to the audible noise that can occur because of the power range that is covered by burst mode operation.

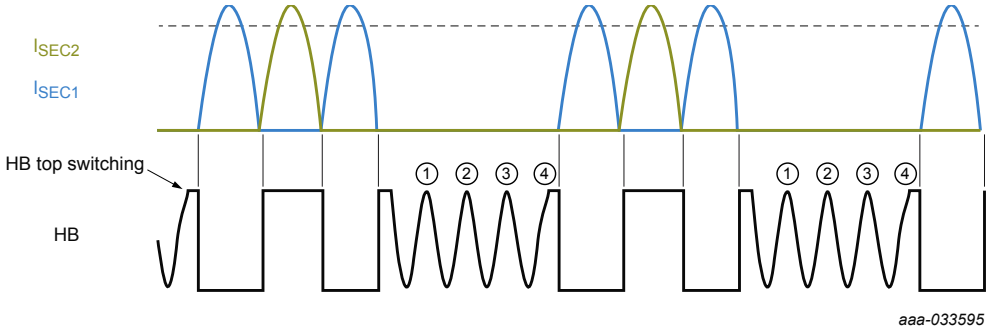
- When the BM repetition frequency is already lower than the preset BM repetition frequency, the BM energy-per-cycle increase helps to reduce the repetition frequency at the lowest load condition.
- A higher value for the minimum cycles in burst mode helps to reduce the repetition frequency at the lowest load condition when the BM repetition frequency is already lower than the preset BM repetition frequency.
- The burst mode transition level defines the power region for burst mode operation. The risk of audible noise is limited to the chosen BM power range.
- When the application has a varying load condition that makes the system continuously switch between BM and LP operation, the LP-BM delay time can help avoid audible noise. The selectable delay time keeps the system in LP mode for a longer time and avoids audible noise during this condition.

The TEA2016AAT also offers an option to disable burst mode operation by the LP-BM delay time option for infinite. For running stable at no load or very low load conditions in LP mode, the Zero Power slope setting helps to optimize the operation for a specific application.

See Section 13.5 for more information on how to use IC functions to reduce audible noise in burst mode operation.

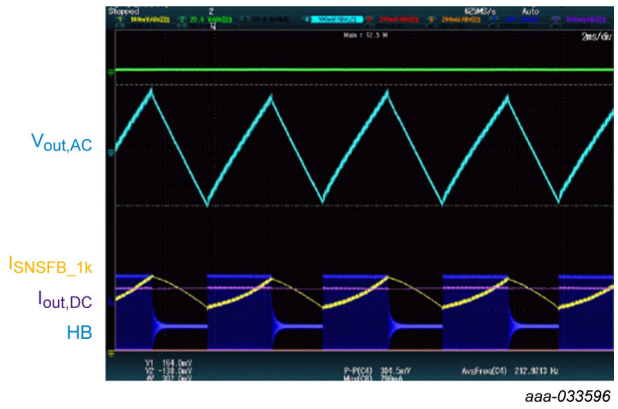


a. LP number of peaks = 2

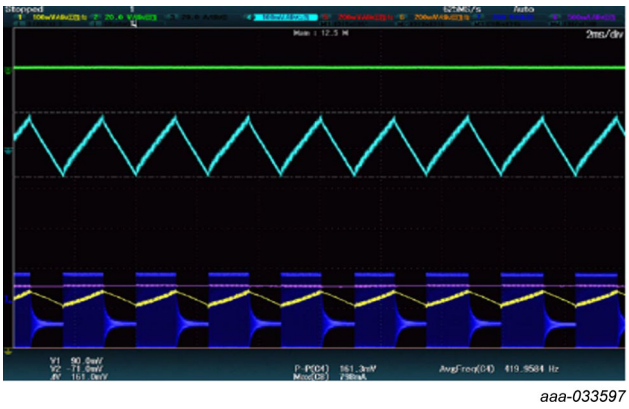


b. LP number of peaks = 4

Figure 61. LP number of peaks



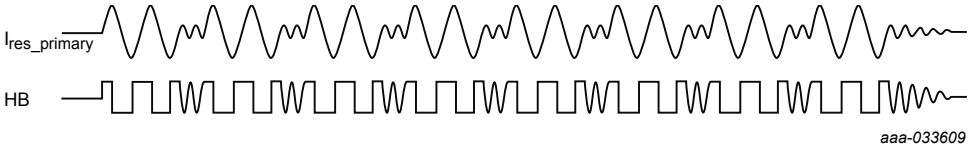
a. BM repetition set to 200 Hz



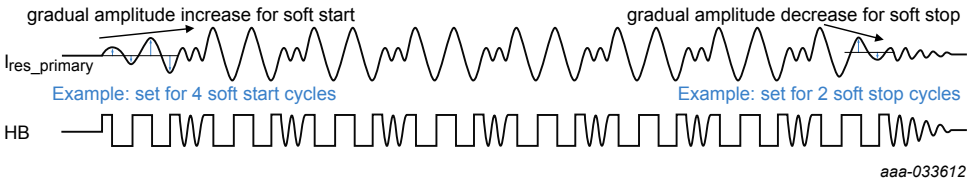
a. BM repetition set to 400 Hz

Maximum output voltage ripple at 50 % duty cycle BM

Figure 62. BM repetition frequency set to 200 Hz and 400 Hz



a. Standard burst sequence



b. Burst sequence with soft start and soft stop

Figure 63. LLC burst mode setting examples for soft start and soft stop

11.3 Measures in the coil and transformer construction

In addition to the methods used in the controller ICs to minimize audible noise, measures in the mechanical construction of the LLC transformer and the PFC coil can be applied.

Often, a varnish is put on the complete transformer to reduce audible noise. It is a commonly used method for systems that apply burst mode operation.

If the windings itself produce noise, filling glue between the windings can be applied. It is not used often because it makes the transformer production more difficult.

To reduce the noise from the core, softer air-gap material can be used. This method is not used often because of the non-standard air-gap material that is necessary.

12 Practical system implementation subjects

12.1 Start-up and debugging

When starting a newly build application or when an error or incorrect behavior is observed during operation, it is possible to simplify analyses by operating the LLC or PFC separately. This option helps to locate errors more easily and makes it possible to do a performance evaluation under conditions that restrict the influences from other circuit parts.

The following sections show several examples of splitting the converters.

12.1.1 LLC only operation with DC boost voltage

There are two options for testing or debugging the LLC converter operation without influence of PFC operation.

- Disable PFC operation using the GUI option: PFC disable.
  With this option, it is easy to observe differences in LLC behavior with or without PFC operation by switching the PFC disable function on and off.
- Disconnect the gate of the PFC MOSFET. Several PFC related functions remain operational.
  To prevent PFC switching, disconnect the pin GATEPFC (pin 5) and short the PFC MOSFET gate to GND.

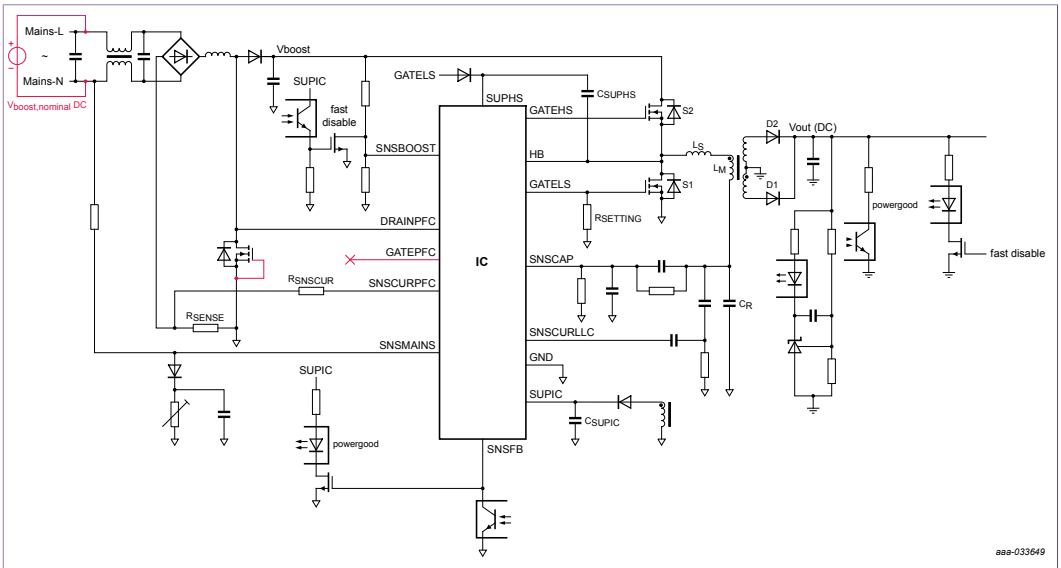


Figure 64. LLC only operation with DC boost voltage

Connect an external DC source to generate V_{boost} (in most cases, it is a value close to 400 V (DC).

In some cases, to observe the LLC behavior, the DC boost voltage can be increased or decreased. In this case, to enable LLC operation at lower boost voltage, an external voltage of 2.5 V can be applied on SNSBOOST. And to supply the IC for operation, an external source of 20 V can be connected to SUPIC.

12.1.2 PFC only operation

For testing and debugging the PFC converter, it can be useful to disable operation of the LLC converter. It can be done with a few (temporary) modifications.

1. Disconnect V_{boost} from the LLC converter
2. Supply SUPIC with approximately 22 V using an external supply.
3. Set OPP timers to infinite (to avoid protection triggering).
4. To simulate that the start-up is finished (SNSFB current flowing), connect a 2.2 kΩ resistor from SNSFB to GND.

To start working and generate 400 V output to V_{boost}, apply the mains voltage to PFC.

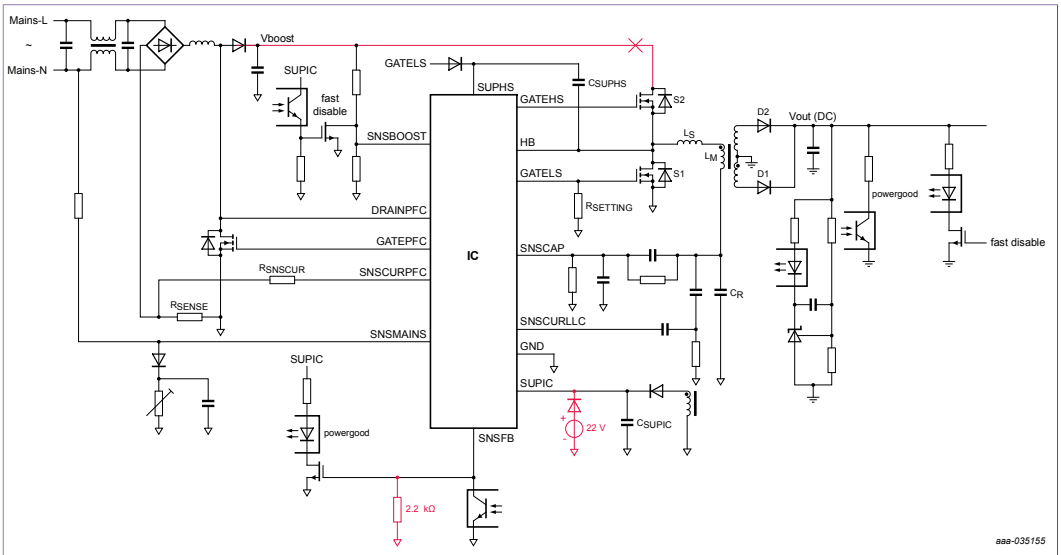


Figure 65. LLC only operation with DC boost voltage

12.1.3 Checking the SNSCAP divider

After implementing the estimated SNSCAP divider values, it is important to check the result to the power limit level in the real application. There may be some application-specific deviations from the values in the estimation. If the power level for power limit is incorrect, the divider values must be corrected for a good result.

By programming an electronic load with a load step sequence, the system can be analyzed in the application (see Figure 66) to check the output voltage dropping at a certain peak load.

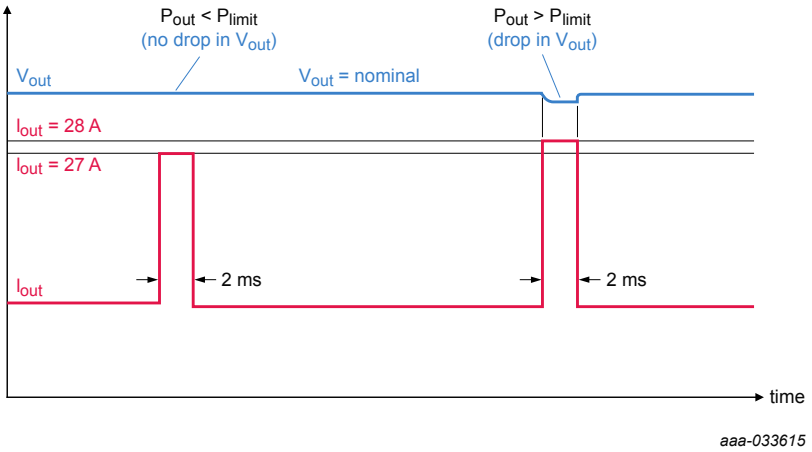


Figure 66. Test power limit level by checking the output voltage dropping

When the measured power limit level is incorrect, the SNSCAP divider must be modified. In practice, a small change in the $C_{SNSCAPlow}$ value can modify it.

Note: *The power limit during this test can temporarily be set to a convenient or important value, for example, 100 % or 140 % (near the intended OPP level). When the SNSCAP divider is correct and the compensation for the power range (see Section 12.1.4) is set, the value necessary for the application requirement can be restored to, for example, 170 %.*

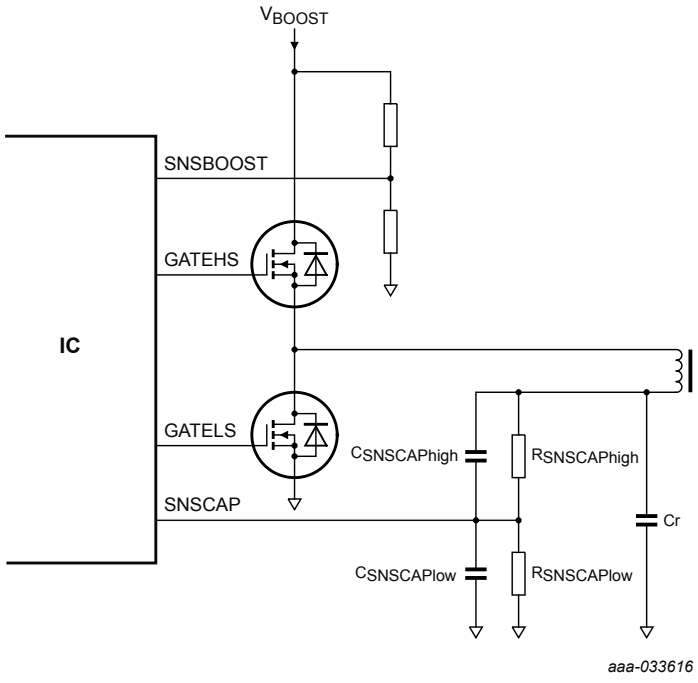


Figure 67. SNSCAP divider

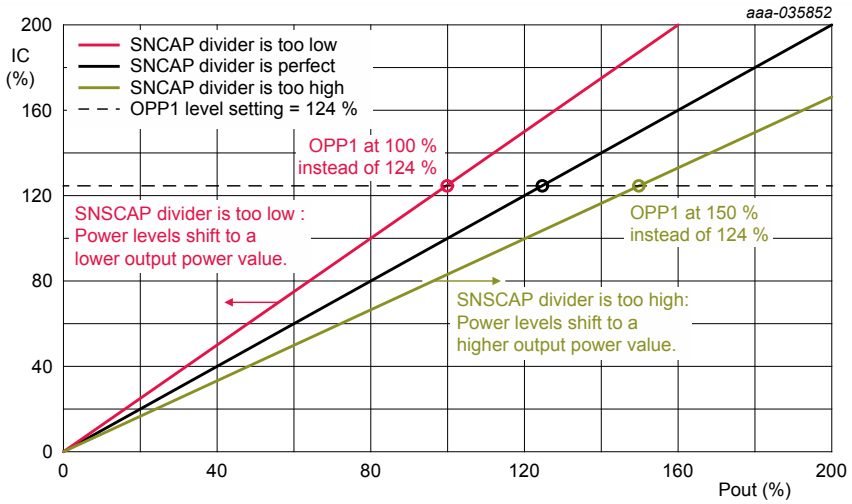


Figure 68. Results of a correct and incorrect SNSCAP divider

12.1.4 Tuning for a correct power range using dVcap offset

After optimizing the SNSCAP divider to match the IC power level percentage for higher values, an extra improvement can be made for lower power levels. It mainly concerns the burst mode transition level. At lower power levels, the time delay in the SNSCAP regulation can result in a difference between the LP-BM transition level selected from the setting and the real power level percentage.

The dVcap offset and ZPS function can help to optimize the basic compensation in the IC for this time delay, which is partly application-dependent (see Section 9.8.1).

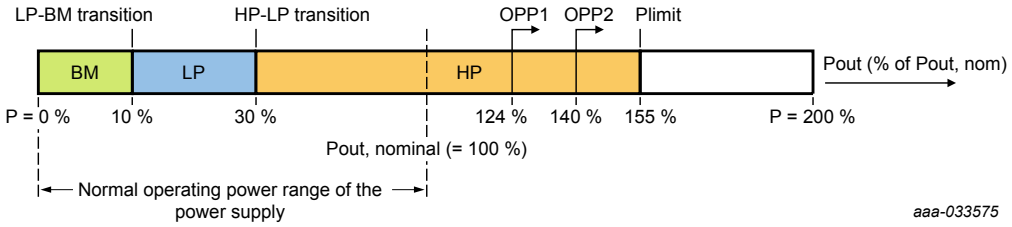


Figure 69. Mode transitions on power scale

After optimizing the SNSCAP divider using a high power level, the mode transitions at lower power levels can be checked: HP-LP and LP-BM. They may show a deviation from the selected value. To obtain the best matching result, you can use the dVcap offset and/or ZPS.

It is not important to have a very good match because transition and protection levels related to the power scale can be tuned independently to obtain the correct result.

The change in ZPS only has a very small effect on higher power levels like the OPP level or the power limit level. It can only decrease the transition levels.

The dVcap offset can also provide a correction to the mode transition levels. A change in dVcap offset has a significant effect on the OPP and power limit levels. The SNSCAP divider must be readjusted.

Rule of thumb:

- **dVcap**:
  - The transition percentage level of BM and HP-LP changes +0.1 % at every +1 mV change of the dVcap level after correcting the SNSCAP divider again.
- **ZPS**:
  - The transition percentage level of BM changes −0.4 % at every +1 mV/µs change of the ZPS after correcting the SNSCAP divider again.
  - The transition percentage level of HP-LP changes −1 % at every +1 mV/µs change of the ZPS after correcting the SNSCAP divider again.

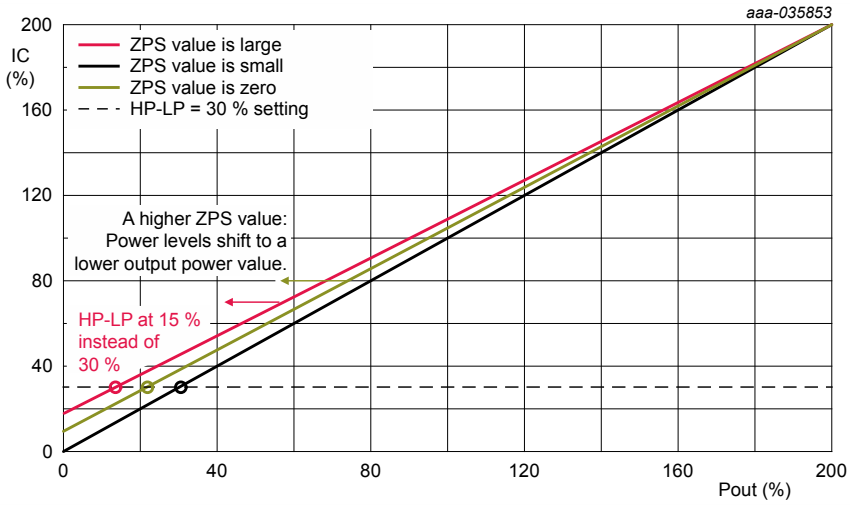


Figure 70. Basic effect on the power levels by the ZPS value

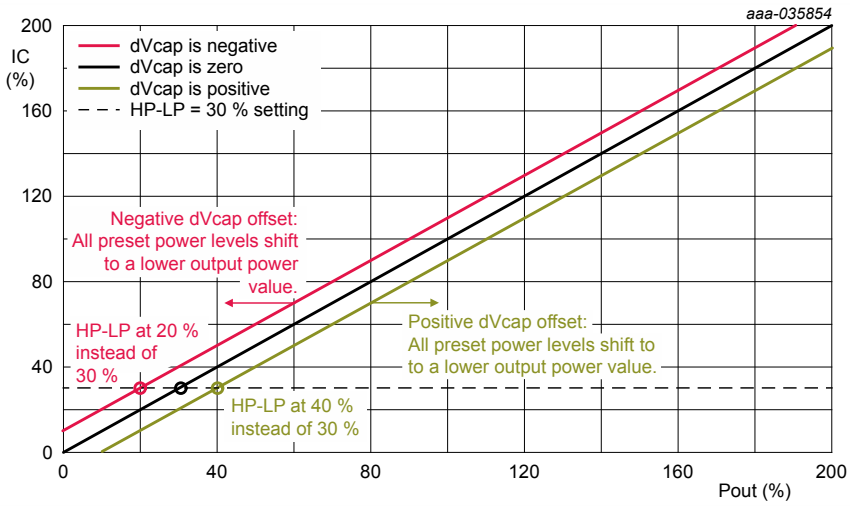


Figure 71. Basic effect on the power levels by the dVcap offset value

12.1.5 Load sweep for checking the mode transitions and behavior

To observe the complete power range of the power supply, it is useful to apply a load sweep from no load to nominal load during a longer time (seconds). In this way, several properties and behavior can be studied in one oscilloscope picture. Several electronic

load devices offer this possibility by connecting a function generator signal to an analog input that drives the current load value.

Subjects that can be checked:

- Regulation instability in certain load conditions
- Mode transitions at the expected or required power levels
- Output ripple voltage according to expectations or higher due to disturbance or instability of operation at certain load conditions.
- Hysteresis at LP/HP transition: different transition levels between increasing and decreasing the output power.

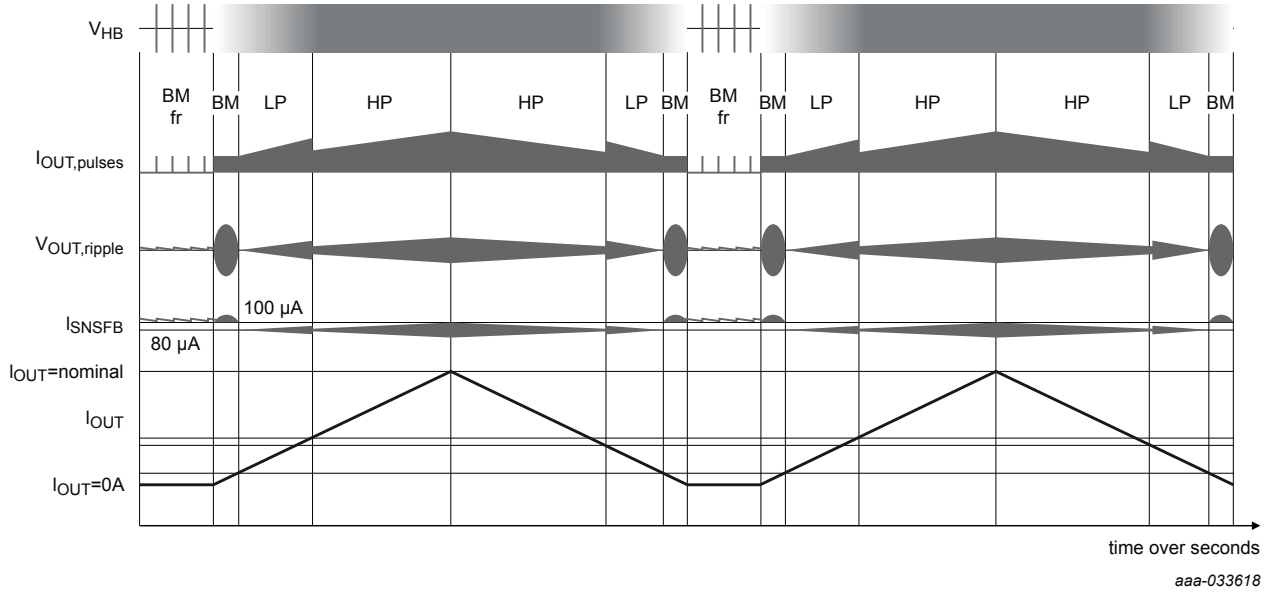


Figure 72. Load sweep for checking the mode transitions and behavior

12.2 Output regulation error amplifier for low current consumption

For low power consumption at low load conditions, the SNSFB regulation can work on a very low current level. The level can be selected using the optocoupler current level parameter.

To make sure that the complete feedback circuit works well at low current levels, the circuit components must be selected.

The error amplifier must be a type for low current consumption. The TEA2016DB1519v2 uses an AS431 that works on a typical current of 50 µA.

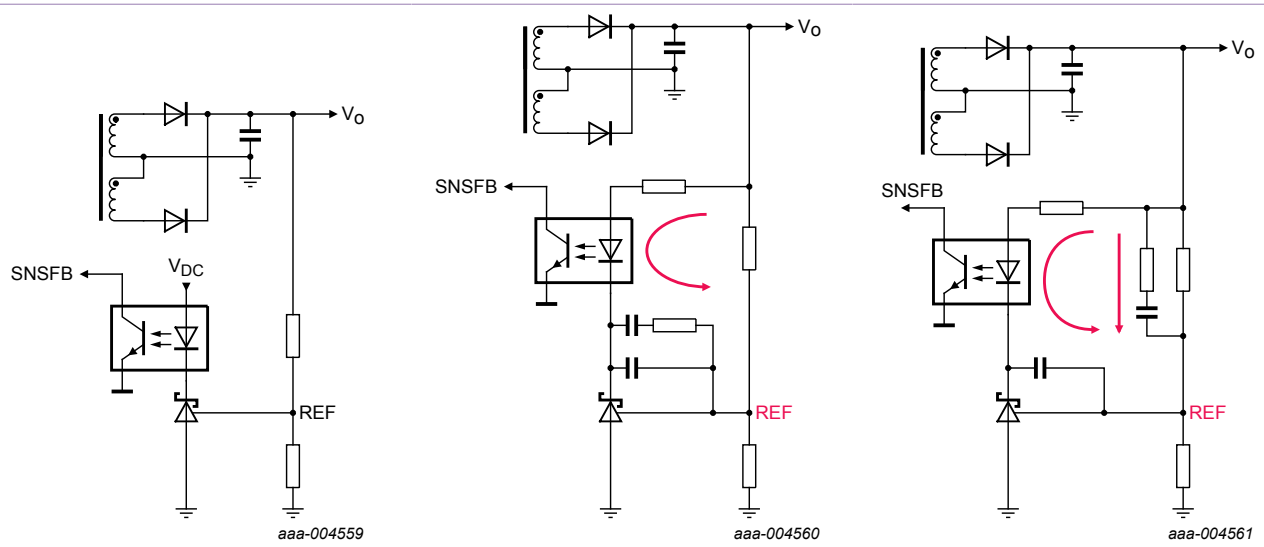
12.3 Output voltage variation because of error amplifier circuit

For good regulation effect during load variations, a capacitive path is often added in the error amplifier circuit. Figure 73 shows the basic circuit and two practical circuit examples. When the capacitive coupled effect is too strong, the capacitive path can have a negative effect on the output voltage increase during start-up. As the voltage on the reference pin increases faster than the real output voltage, the error amplifier concludes that the nominal output voltage is reached before it actually is. It reacts by reducing the amount of output power via the feedback signal. The effect is that the output voltage increase shows a hiccup (see Figure 74).

Using the capacitive feedback in a moderate way can prevent this problem.

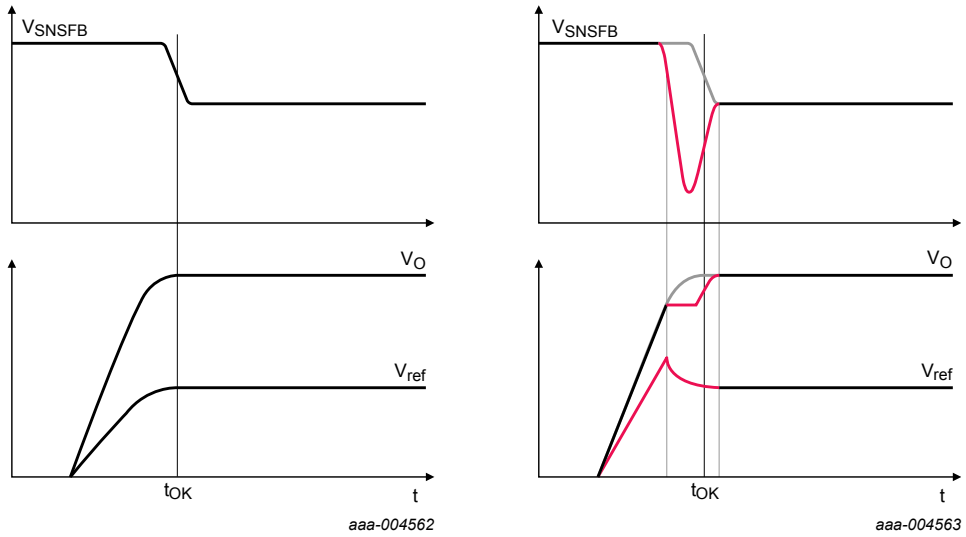
The value of the capacitor and the value of a possible series resistor determine the capacitive feedback.

A trade-off between the dynamic behavior (load variations and burst mode operation) and the start-up behavior can be required.



a. Principal feedback circuit b. Practical example circuit 1 c. Practical example circuit 2

Figure 73. Examples of two feedback circuits that use a capacitive path



a. Proper start-up behavior

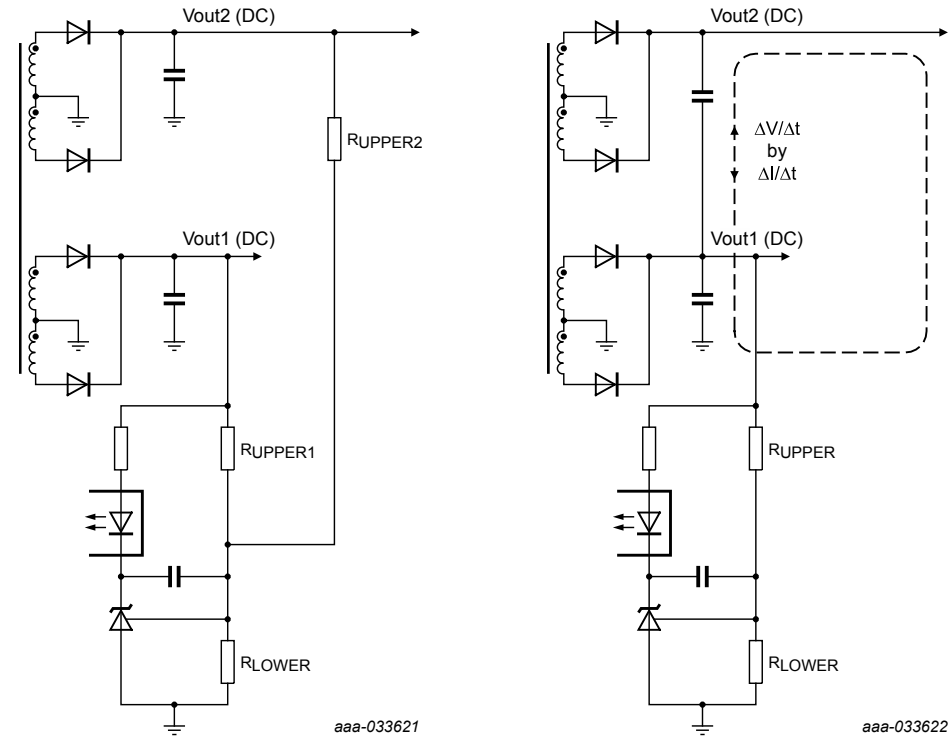
b. Wrong start-up behavior because of the effect of the capacitive path being too strong

Figure 74. Good and bad start-up behavior by regulation

12.4 Converter with two output voltages

In some applications, two output voltages are required. Typical for TV applications is the requirement of a high output voltage for LED backlight power in addition to the lower (12 V) supply voltage.

Sometimes, there can be regulation issues during load step testing because it is not possible to regulate two output voltages.



a. Split feedback

b. Capacitive coupling of outputs

Figure 75. Two methods of improving 2 output behavior by 1 feedback

12.4.1 Two output voltage regulation by shared feedback

For regulating two output voltages, the output voltage sensing can be split up (see circuit Figure 75(a)). The upper resistor of the voltage divider can be split into R_{UPPER1} to V_{OUT1} and R_{UPPER2} to V_{OUT2}.

Tthe values of R_{UPPER1} and R_{UPPER2} can choose the contribution of each output. Often one of the outputs is more important or critical than the other.

A disadvantage of this type of regulation is that the load of each output changes the output voltage of the other output.

Calculation example:

- V_{OUT1} = 13 V
- V_{OUT2} = 160 V
- $V_{REFERENCE\_ERROR\_AMPLIFIER}$ = 2.5 V
- R_{LOWER} = 10 kΩ

$$I_{LOWER} = I_{TOTAL} = 2.5\ V\ /\ 10\ k\Omega = 0.25\ mA$$

The choice of the resistor value for R_{UPPER1} or R_{UPPER2} must be close to the value for single output regulation but a little higher to find a solution.

For a single output regulation R_{UPPER1} should be:

$$R_{UPPER1} = \left(V_{OUT1} - V_{REFERENCE\_ERROR\_AMPLIFIER}\right) / I_{TOTAL} = 13\ V - 0.25\ mA = 42\ k\Omega$$

For split regulation, the value for R_{UPPER1} must be higher, for example, 51 kΩ.

When R_{UPPER1} = 51 kΩ, the current from the 13 V is:

$$I_{VOUT1} = (13\ V\ -\ 2.5\ V)\ /\ 51\ k\Omega = 0.206\ mA$$

The remaining current must flow from the 160 V output:

$$I_{VOUT2} = 0.25\ mA\ -\ 0.206\ mA = 0.044\ mA$$

$$R_{UPPER2} = (V_{OUT2}\ -\ V_{REFERENCE\_ERROR\_AMPLIFIER})\ /\ I_{VOUT2} = (160\ V\ -2.5\ V)\ /\ 0.044\ mA = 3570\ k\Omega\ (3.6\ M\Omega)$$

With these example values, the regulation contribution of each output is:

$$V_{OUT1}: 100 \times I_{VOUT1}\ /\ I_{TOTAL} = 100 \times 0.206\ mA\ /\ 0.25\ mA = 82.4\ \%$$

$$V_{OUT2}: 100 \times I_{VOUT2}\ /\ I_{TOTAL} = 100 \times 0.044\ mA\ /\ 0.25\ mA = 17.6\ \%$$

12.4.2 Output voltage coupling using an output capacitor

It is also possible to regulate the main output voltage only and connect the other output voltage to it with the output capacitor (see Figure 75(b)).

The current from a voltage change through the capacitor of the unregulated output also flows through the capacitor of the regulated output. Voltage variations on the unregulated output, during load steps, for example, now have a similar effect on the regulated output. The feedback regulation for constant output voltage corrects for variations and indirectly also regulates the unregulated output voltage.

The steady state behavior is not compensated because the coupling using the capacitors only shows the variations in current or voltage.

12.5 SNSBOOST disable function

The system operation can be stopped by pulling down SNSBOOST. The behavior of the fast disable function can be determined with parameter settings:

- On/off: When SNSBOOST becomes low, the system stops operation immediately. When SNSBOOST is released, the system restarts.
- Safe restart: When SNSBOOST becomes low, the system operation stops immediately. Follow-up with safe restart until SNSBOOST is released.
- Latched: When SNSBOOST becomes low, the system operation stops immediately. Follow-up with a latched protection.

Option 1 is typically used for a standby function in a system with a separate standby supply. An accurate secondary output sensing circuit typically uses options 2 and 3 for protection.

Table 8. SNSBOOST fast disable function

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{scp(stop)}$	stop short-circuit protection voltage		0.37	0.39	0.41	V
$V_{scp(start)}$	start short-circuit protection voltage		0.40	0.45	0.50	V

It is important that the voltage on SNSBOOST is pulled down (and released) fast, to avoid PFC regulation problems. Figure 76 shows an example using a MOSFET on

SNSBOOST to implement a protection. A secondary sensing circuit activates this protection.

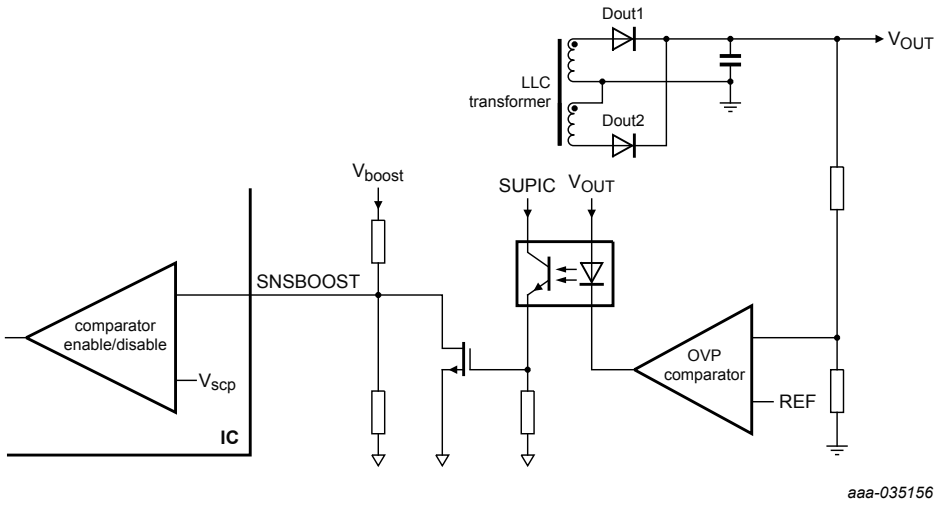


Figure 76. Fast disable function operated by a secondary output OVP sensing circuit

12.6 SUPIC by separate standby power supply

In a system that uses a separate standby power supply, the SNSBOOST enable/disable function can be used for switching on/off the main power supply.

If the separate standby power supply supplies SUPIC, the 12 V SUPIC start level option can be selected.

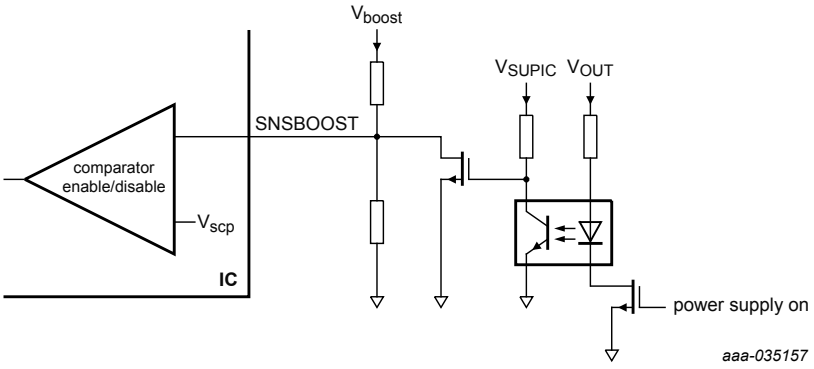


Figure 77. PSON

12.7 Checking limiting values in an application

Checking the condition on an IC-pin in a running application can be difficult because of disturbances. Normally, to see if a voltage on a pin does not exceed the limiting value, an oscilloscope with a voltage probe is used. Because of switching disturbances, the measurement can easily show a voltage that is probably not on the pin but added by the probe. Or the connection of the probe adds energy to the application like an antenna. Both undesired effects show a higher voltage level than there is in reality.

To minimize errors in the measurement, it is important to minimize:

- The influence of connecting a voltage probe to the circuit (add energy to application)
- A voltage added to the measurement by the voltage probe (add signal to real signal)

12.7.1 Measuring advice

To minimize disturbance to the measurement by the voltage probe itself, it is important to minimize the measurement loop signal-to-ground. Figure 78 shows a manually modified probe connection for this purpose.

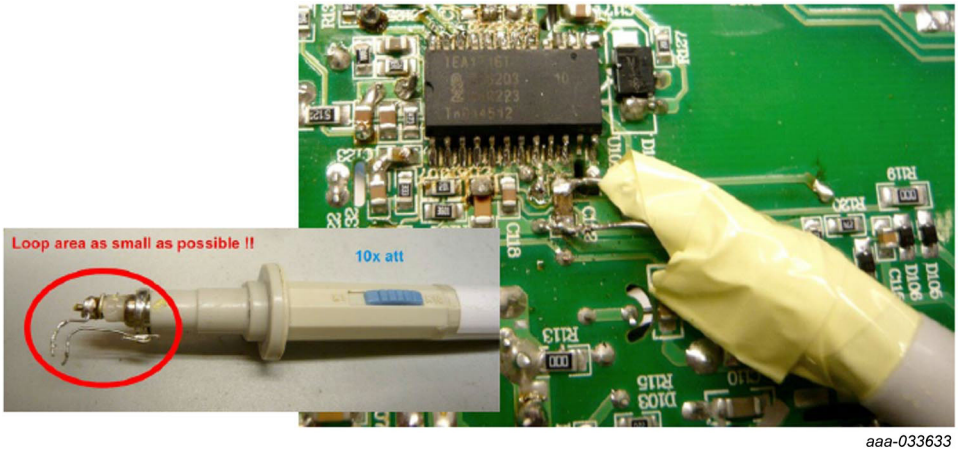


Figure 78. Manually modified probe connection to minimize disturbance to the measurement

Even when taking great care of the measurement setup, some disturbance still occurs in most measurements. In some cases, it is difficult or impossible to prove that the application is within the limiting values. In such a situation, additional measurements can help to obtain more information on what is really happening. In such cases, engineering judgment is required to decide, based on the collected information, if the application is OK or if a problem must be solved.

12.7.1.1 Estimation of the amount of signal added when using a voltage probe

To get an indication on which part of the measurement result the voltage probe adds, a reference measurement can be done by connecting the probe to the ground connection of the probe.

The signal that appears on the oscilloscope is similar to the signal that is added to the original measurement.

To reduce the amount of disturbance in the measurement, consider using a bandwidth limiting function on the oscilloscope. For most measurements, a signal bandwidth of 20 MHz is sufficient.

12.7.1.2 Adding a peak rectifier circuit to the measurement probe

To indicate if there are voltage peaks on a pin that are too high, a peak rectifier circuit can be added temporarily.

The voltage measured on the capacitor is always lower than the peak voltage on the pin because of the forward voltage of the diode. So, if the voltage on the capacitor exceeds the limiting value, it is an indication that the peak voltages are too high.

The capacitor can have a value of 1 nF. The impedance of the voltage probe, 10 MΩ for example, causes a moderate capacitor discharge to be present.

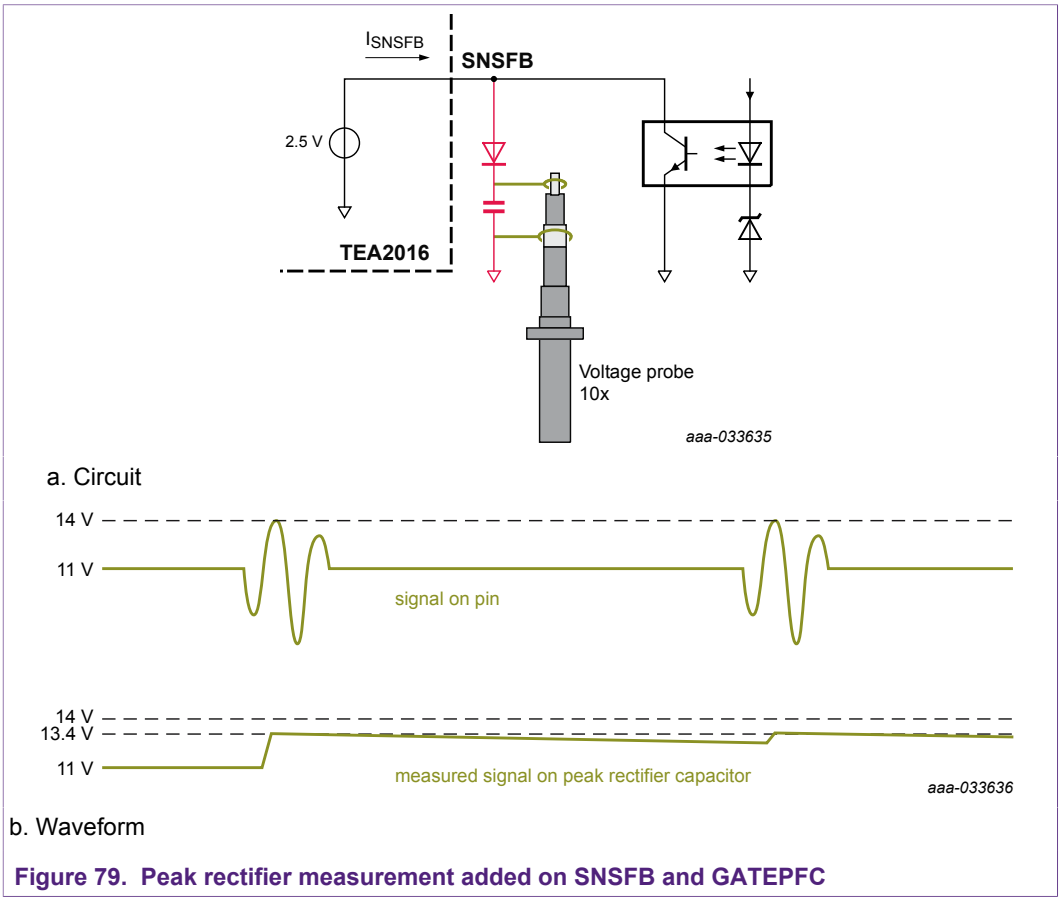


Figure 79. Peak rectifier measurement added on SNSFB and GATEPFC

12.7.2 $V_{SNSMAINS}$ limiting values

$-0.4\ V < V_{SNSMAINS} < +12\ V$

Because SNSMAINS is connected to the mains voltage with a high impedance (10 MΩ or 20 MΩ), connecting a voltage probe slightly influences the mains measurements. It is not directly a problem because operation normally continues in a similar way. The measurement can be done according to the advice provided in Section 12.7.1.

12.7.3 $V_{SNSBOOST}$ limiting values

$-0.4\ V < V_{SNSBOOST} < +12\ V$

Normally, sufficient decoupling is in place because of a capacitor on SNSBOOST. When applying the advice provided in Section 12.7.1, the measurement itself is not critical.

If the PFC loop regulation stability is critical or a long track is connected, a measurement with a voltage probe can disturb the PFC operation. Because the PFC regulation is at 2.5 V and a capacitor of several nanofarads is connected, the limiting values of this pin are not expected to be critical.

12.7.4 $V_{SNSCURPFC}$ limiting values

$-0.4\ V < V_{SNSCURPFC} < +12\ V$

The measurement can be done applying the advice provided in Section 12.7.1. The measurement itself can be difficult because of the PFC switching which can disturb the measurement result.

Although the measured signal for this pin comes from a very low impedance resistor, there is a risk of negative voltage spikes because of the high current levels and the PFC MOSFET switching. Also, if a PCB layout grounding problem occurs, high converter currents through ground tracks can add a signal to SNSCURPFC. To limit the current in the IC circuits, an external series resistor must be added.

The most critical situation is expected at start-up because of the high inrush current that charges the V_{boost} capacitor. A similar situation occurs during surge (test) conditions. During operation, low mains voltage and high output power can cause the voltage levels to become too low.

12.7.5 V_{SUPHS}, V_{HB}, V_{GATEHS}, V_{GATELS}, and $V_{GATEPFC}$ limiting values

In Section 7.5 and Section 7.6, the specific situations for GATEPFC, GATELS, GATEHS, HB, and SUPHS are discussed.

12.7.6 $V_{DRAINPFC}$ limiting values

$-0.4\ V < V_{DRAINPFC} < +685\ V$

12.7.7 V_{SUPIC} limiting values

$-0.4\ V < V_{SUPIC} < +36\ V$

Normally, sufficient decoupling is in place because of capacitors on SUPIC. When applying the advice provided in Section 12.7.1, the measurement itself is not critical.

Often, an auxiliary winding on the LLC transformer generates the SUPIC voltage. Depending on the design, when the output power changes, this voltage level can vary. Check the voltage at different load conditions.

Transients can also make the SUPIC voltage vary temporarily. Check load step conditions and the situation at start-up and stopping also.

12.7.8 V_{SNSCAP} limiting values

$-0.4\ V < V_{SNSCAP} < +12\ V$

Normally, sufficient decoupling is in place because of the capacitor on SNSCAP. When applying the advice provided in Section 12.7.1, the measurement itself is not critical.

An internal bias source puts the input signal on a DC voltage level of 2.5 V. The voltage reserve on SNSCAP to the limiting values is high. So, it is not expected to be critical. Check V_{SNSCAP} at mains switch-off.

12.7.9 $V_{SNSCURLLC}$ limiting values

$-0.4\ V < V_{SNSCURLLC} < +12\ V$

The voltage on this pin is a bit difficult to measure because attaching a probe can cause disturbance in operation. An internal bias source puts the input signal on a DC voltage level of 2.5 V. A capacitor connects the AC voltage that represents the resonant current signal to this pin. The AC voltage part can best be checked on the measurement resistor. When applying the advice provided in Section 12.7.1, this measurement is not critical.

The voltage reserve on SNSCURLLC to the limiting values is high. So, it is not expected to be critical.

If measurement on the pin itself is required, consider using the rectifier method to observe the behavior.

12.7.10 V_{SNSFB} limiting values

$-0.4\ V < V_{SNSFB} < +12\ V$

Because the SNSFB function is current-controlled at a relative low voltage during operation with only an optocoupler connected, the risk of reaching limiting values is very low.

When generating the power good signal, the voltage is increased and decreased slowly (selectable 1 ms to 4 ms) with a minimum risk of overshoot or undershoot when only a MOSFET gate is connected. Additional circuits connected may increase the risk.

When applying the advice provided in Section 12.7.1, the measurement itself is not critical.

12.8 Measurements in no-load condition

To observe and measure performance during no-load operation, it is important to remove the I^2C communication. The I^2C communication prevents that the TEA2016AAT IC enters low-current consumption state.

Minimize the amount of equipment and probes connected. They can influence the performance through additional parasitic elements.

Using an electronic mains supply can have a different result than using a mains connection with a (variable) mains transformer. To avoid regulation issues or limitations in an electronic source, a transformer is preferred.

It can take several minutes until operation in no load is in stable regulation.

13 Using setting parameters to optimize behavior and performance

13.1 Proposed way of working

To optimize several performance aspects, the TEA2016AAT offers many parameters. It is important to get familiar with the available options and identify the groups of parameters that belong to a certain function or performance aspect. By modifying them during operation and observing the resulting behavior and performance, provide a good understanding of how to use them.

General guidelines

- Start with the default IC settings. The default IC settings are middle of the road settings for power supplies.
- You can save the initial settings as a .mif file for backup. And save several intermediate versions for reference on changes you made.
- Modify only parameters that improve the performance as required. Try to minimize the number of setting changes and modify them in a moderate way. Only make extreme changes if it is necessary and you understand the consequences.
- Identify the group of parameters that influences the performance testing you are doing. Include the circuit design aspects like related component values. The sections in this application note and the info pop-up in the GUI can be helpful.
- Check if parameter changes affect other performance aspects. Usually, the info pop-up in the GUI and the corresponding section in this application note mention possible side effects.
- Do a review at the end of a job. To see if there is a parameter that was changed accidentally, compare the list of default settings with the modified list.

13.2 Making the best choice for low load (BM) operation

At low output load, there are 3 performance subjects that are related by design choices that are made. Sometimes a compromise must be chosen.

- Efficiency or power consumption (Section 13.3)
- Output voltage ripple (Section 13.4)
- Audible noise (Section 13.5).

In the following sections they are discussed separately, but including the effect on the other performance subjects. Many relevant settings influence all 3 subjects. A certain choice can give an improvement for one performance subject but reduces the performance of another subject.

13.3 Increase efficiency at low-load conditions

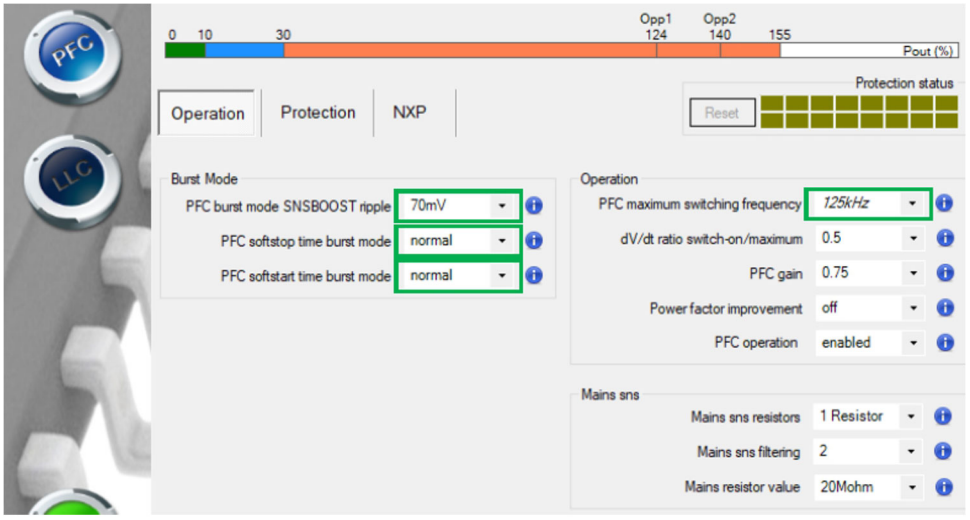


Figure 80. PFC-related parameters that can help to increase low-load efficiency

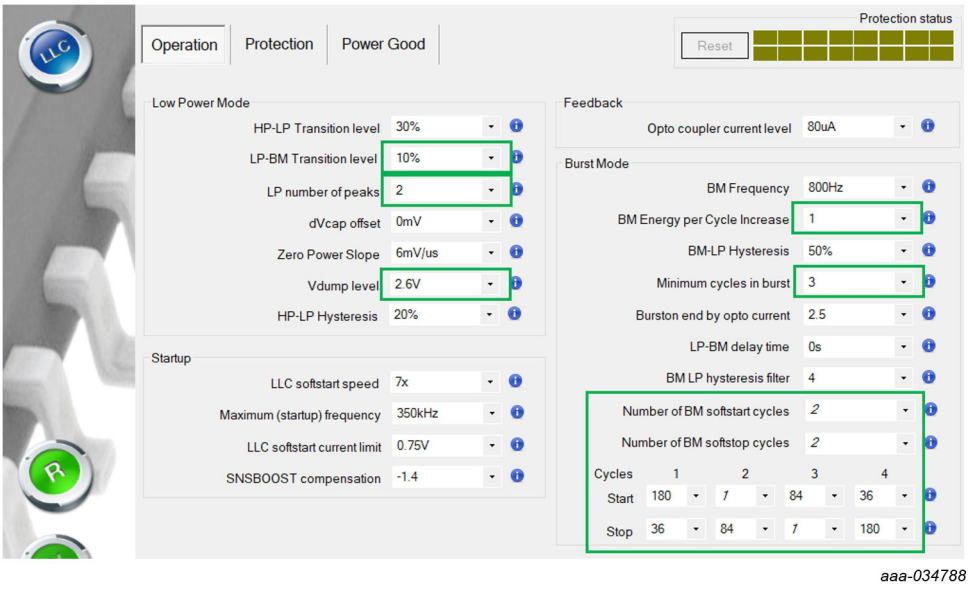


Figure 81. LLC-related parameters that can help to increase low-load efficiency

13.3.1 PFC burst mode SNSBOOST ripple

The PFC can operate in two types of burst mode. The type can be selected using the PFC burst mode SNSBOOST ripple setting.

Figure 82 shows the two types of PFC burst mode the behavior of the PFC in burst mode.

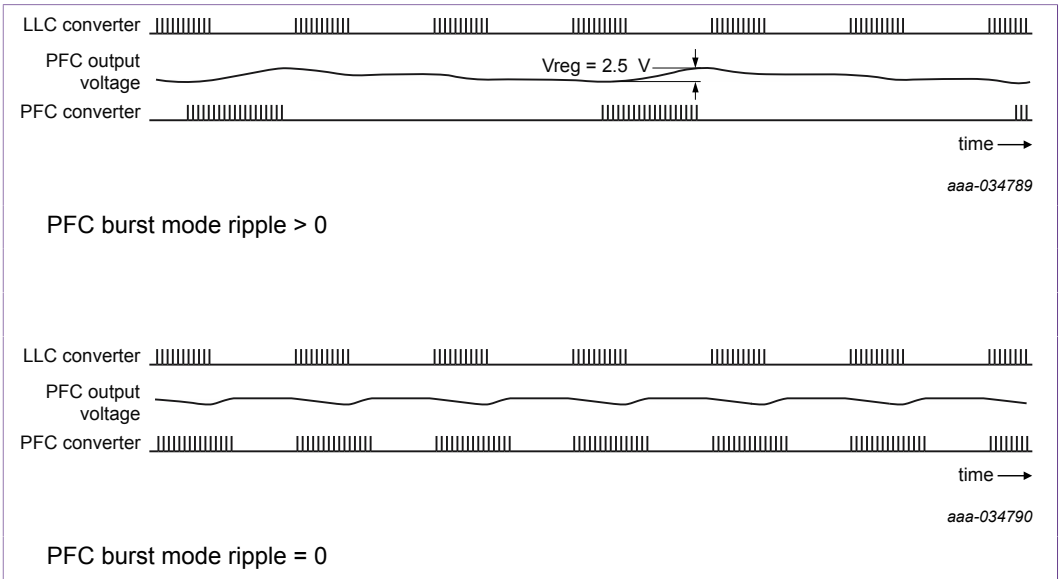


Figure 82. PFC burst mode based on output voltage ripple or synchronous with LLC burst

The best setting for efficiency at low loads in general is to apply the largest ripple. It reduces the number of bursts in time.

At no load, there is no significant difference between burst types. However, at higher power levels in BM the efficiency increases.

PFC burst mode operation is only active when the LLC burst duty cycle is smaller than 50 % (lowest power range).

The effect on the LLC output voltage ripple is negligible.

The effect on audible noise is limited. It must be tested with a practical application.

13.3.2 PFC soft start and soft stop

To reduce the audible noise from the PFC coil, a soft start and/or soft stop can be added to the PFC burst. However, it can lower the efficiency because several switching cycles hardly produce output power while there are switching losses.

Best setting for efficiency is to disable both soft start and soft stop (select “no”).

The effect on LLC output voltage ripple is negligible.

Adding soft start and soft stop slightly increases the power consumption. When using an output voltage ripple setting > 0, the effect is almost negligible.

13.3.3 PFC maximum switching frequency

This switching frequency limit is intended to reduce switching losses at low output power conditions for a better efficiency. The best setting for efficiency is for a low frequency.

The effect of this parameter setting on audible noise and LLC output voltage ripple is negligible. However, a lower frequency limit reduces the power factor and the THD performance. A trade-off must be made between these performance subjects.

13.3.4 LLC LP number of peaks

The BM consists of series of LP cycles. So, the definition of the LP cycles also influences the BM performance.

The low-power mode increases the efficiency in the power range between high-power mode and bust mode operation. It combines the benefits of HP and BM. It is a kind of mini burst mode at higher power levels and reduces the number of switching cycles. In time, reducing the switching cycles reduces the switching losses. And puts a higher energy in the remaining cycles to have the same output power.

The LP number of peaks defines the duration of the period of not switching. A higher value results in a longer period of not switching, which the IC compensates with a higher energy-per-cycle during the period of switching.

Increasing the number of peaks, increases the efficiency. However, the LP period becomes longer and the LP repetition frequency can enter the audible range below 20 kHz.

When the LP period is longer, the output voltage ripple increases. However, normally, the ripple is not critical in the LP range and remains lower than in BM or at the highest load in HP.

13.3.5 V_{dump} level

The BM consists of series of LP cycles. So, the definition of the LP cycles also influences the BM performance.

The V_{dump} level can be used to optimize the LP mode switching in a specific application further. It can also be used to find the best result for three equal output current pulses and no current to the output during the non-switching period. In most cases, optimizing to get the best efficiency is more important than obtaining the best looking switching sequence on the oscilloscope.

13.3.6 LLC LP-BM transition level and BM energy-per-cycle increase

The LP-BM transition level parameter setting defines the power range that operates in BM. The use of BM operation increases the efficiency at low power levels by introducing periods of not switching and concentrating the required power in a shorter period of power conversion. It saves the basic losses during the period of not switching.

Make a selection for the transition level that fits best to the application requirement at low load conditions (no-load condition or standby condition).

Energy-per-cycle

The transition level also determines the energy-per-cycle in BM. A higher LP-BM transition level results in a higher energy-per-cycle and increases the efficiency. A higher energy-per-cycle for a higher efficiency can also be obtained using the BM energy-per-

cycle increase setting. This setting can be used to increase the efficiency even further without changing the BM transition level.

The output voltage ripple increases because of a higher energy per cycle. when the BM mode is left and the LP mode is entered, the setting for BM-LP hysteresis influences the highest ripple value.

The audible noise improves in the lowest load area because the result of a higher energy-per-cycle is a lower burst repetition frequency.

13.3.7 LLC minimum cycles in BM

Normally, in BM operation, the system regulates to a preset burst repetition frequency for a predictable result on audible noise. To regulate the power when the output power becomes lower, it reduces the number of LP pulses in each burst. However, when the number of pulses reaches the selected minimum amount, the repetition frequency is reduced to obtain a power reduction.

In the lowest power range, the setting of the minimum number of cycles contributes to the amount of energy in each burst.

A higher value for the minimum cycles in BM increases the efficiency at certain power levels and reduces audible noise because of a lower repetition frequency. However, the output voltage ripple increases.

13.3.8 LLC soft start and soft stop

The LLC soft start and soft stop features reduce audible noise. However, adding a few extra cycles, that do not provide much output current, reduces the efficiency.

The best compromise is usually to use a basic soft start and soft stop (two cycles) where only the very first and very last settings reduce the current. The remaining cycles provide the same current as the remaining LP cycles in the burst. It gives a good improvement on audible noise and minimizes the reduction of efficiency.

The LLC soft start and soft stop features have a minor effect on the output voltage ripple.

13.4 Reduce output voltage ripple in BM

In most applications, the amount of output voltage ripple depends on LLC converter functions and is not related to PFC operation. In most designs, the maximum ripple voltage is expected in burst mode operation at a 50 % duty cycle. Or it is expected at maximum output power in HP mode, when BM operation has been optimized for low output voltage ripple.

Because the BM system works with a selectable repetition frequency, the resulting output voltage ripple is directly related to the output capacitor value.

Figure 83 gives a general impression on the amount of output voltage ripple at different output load conditions.

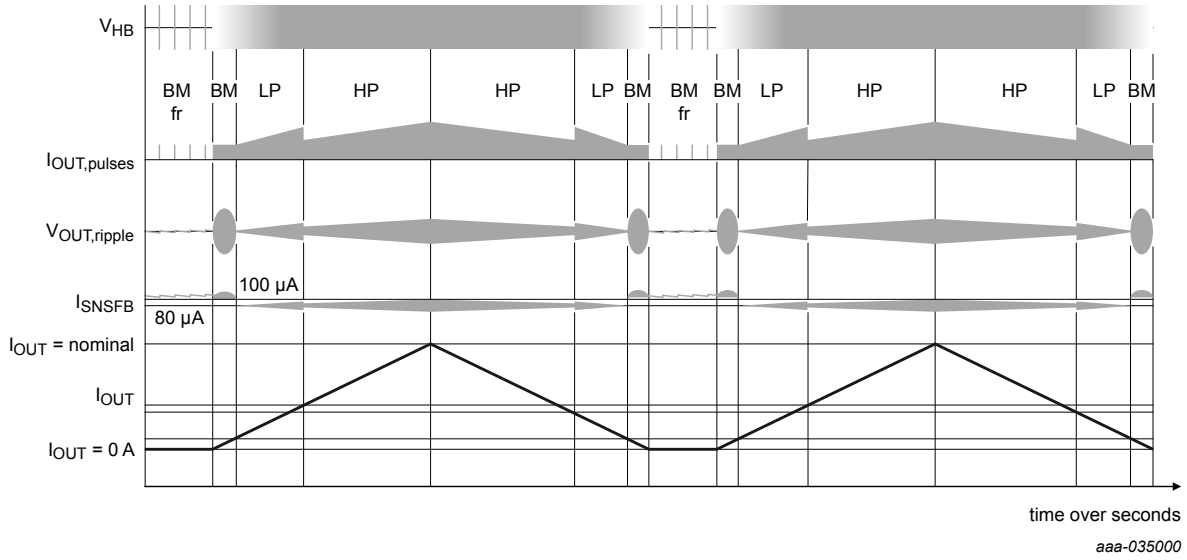


Figure 83. A load-sweep showing typical output voltage ripple behavior at different output load conditions

The output power (or output current) level at which the BM switches at a 50 % duty cycle level, depends on the selected LP-BM transition level and the selected BM energy-per-cycle Increase value.

The 50 % duty cycle power level can be calculated:

$$I_{BM\_50\%dc} = \left(LP - BM\right) \times I_{out(100\%)} \times BM\ ECincr \times dc \tag{21}$$

Example:

- $I_{out(100\%)}$ = 20 A
- LP-BM level = 10 %
- BM ECincr = 1

$$I_{BM\_50\%dc} = 10\ \% \times 20\ A \times 1 \times 50\ \% = 1\ A$$

If the 50 % duty cycle situation is reached at higher value settings of BM ECincr It, depends on the BM-LP hysteresis setting. At a higher energy-per-cycle condition, the system runs at a lower duty cycle, delivering the energy in a shorter time with fewer cycles. When the 50 % duty cycle is not reached, the maximum output voltage ripple occurs at the highest duty cycle condition (see Section 13.4.5).

The output voltage ripple can be calculated:

$$V_{out(pp)} = I_{out} \times \left(1 - dc\right) \times t_{BM} \ / \ C_{out} \tag{22}$$

Example:

- $I_{BM\_50\%dc}$ = 1 A
- duty cycle (dc) = 0.5
- t_{BM} = 1/800 Hz = 1.25 ms
- C_{out} = 3 × 2200 µF = 6600 µF

$$V_{out(pp)} = 1\ A\ \times \left(1\ -\ 0.5\right)\ \times\ 1.25\ ms\ /\ 6600\ \mu F = 95\ mV$$

At BM ECincr = 2, the maximum output voltage ripple is 2× higher.

At BM ECincr = 4, the maximum output voltage ripple can be 4× higher, but it only happens when the hysteresis is set to 100 %.

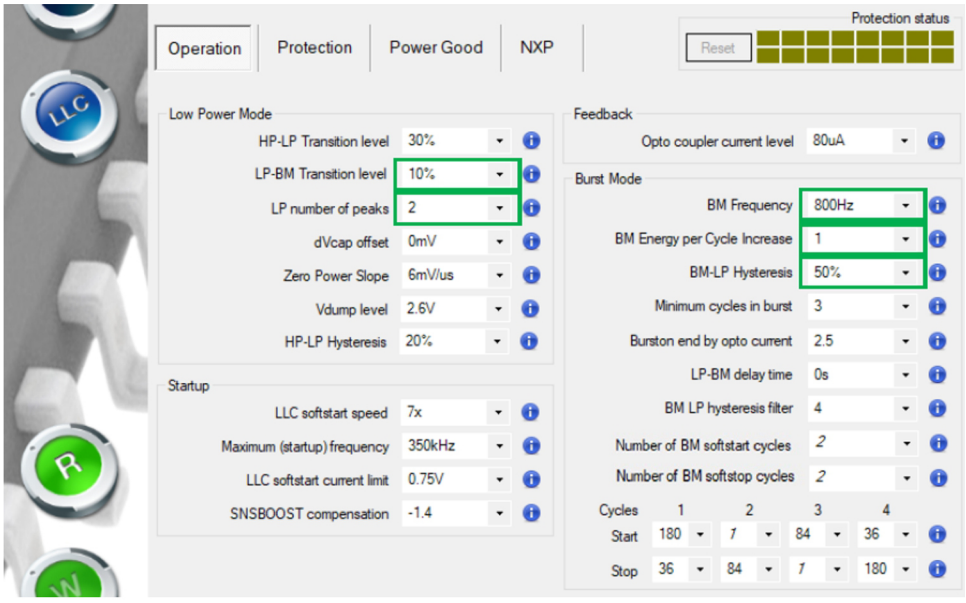


Figure 84. LLC-related parameters that can help to reduce output voltage ripple

13.4.1 LLC LP-BM transition level and BM energy-per-cycle increase

Using BM operation increases the efficiency at low power levels because periods of not switching are introduced and the required power is concentrated in a shorter period of power conversion. It saves the basic losses during the period of not switching. But it also introduces an output voltage ripple. The voltage increases during the burst and drops during the period of not switching.

The LP-BM transition level parameter setting defines the power range that operates in BM. The transition level also determines the energy-per-cycle in BM. A higher LP-BM transition level results in a higher energy-per-cycle and increases the efficiency. The BM energy-per-cycle increase setting can also obtain a higher energy-per-cycle for a higher efficiency. However, the energy-per-cycle increase also causes the amount of output voltage ripple to increase (see calculation examples in Section 13.4).

A lower LP-BM transition level reduces the output voltage ripple.

A lower EC increase reduces the output voltage ripple.

A compromise must be found between efficiency requirements and output voltage ripple.

13.4.2 LP number of peaks

The low-power mode is a kind of burst mode at high repetition frequency. To provide a better conversion efficiency. In this mode, the energy in each pulse is kept relatively high.

During the non-switching period, the losses are low. The number of peaks that is skipped before starting a new LP cycle can set the period of non-switching.

Similar to BM operation, the LP mode increases the output voltage ripple. However, the resulting ripple increase is much lower than in BM. The number of peaks influence the LP output voltage ripple.

Because BM operation consists of series of LP cycles, the LP number of peaks setting slightly influences the total amount of output voltage ripple in BM operation.

A lower LP number of peaks value reduces the output voltage ripple.

13.4.3 BM repetition frequency

The setting of the BM repetition frequency has a major influence on the output voltage ripple. It determines the time that the output voltage increases and decreases. A longer time results in a higher output voltage ripple amplitude.

A higher BM frequency value reduces the output voltage ripple. However, a higher BM frequency also increases the risk of audible noise.

13.4.4 Output voltage capacitor value

Because the BM system works with a selectable repetition frequency, the resulting output voltage ripple ìs directly related to the output capacitor value. A higher value of the output capacitors reduces the output voltage ripple.

13.4.5 BM energy-per-cycle increase behavior with BM-LP hysteresis

A higher value of the energy-per-cycle increase parameter increases the output voltage ripple. When the power increases, the BM-LP hysteresis increases the power range of the BM operation. The maximum output voltage ripple is the same for all hysteresis settings.

Figure 85 shows the resulting behavior.

For reference, Figure 85 (left side) shows a BM energy-per-cycle increase = 1 measurement. In this condition, no transition hysteresis is necessary.

When the BM energy-per-cycle increase value is greater than 1, the BM-to-LP transition level can be calculated:

BM − LP = LP − BM level × (100 % + BM − LP hysteresis)

Example:

BM − LP = 10 % × (100 % + 25 %) = 10 % × 1.25 = 12.5 %

Table 9. Example for the resulting transition level from BM to LP

See Figure 85

LP-BM level (%)	BM energy-per-cycle increase	BM-LP hysteresis (%)	resulting BM-LP level (%)
10	1	50	10
10	2	25	12.5
10	2	50	15
10	2	75	17.5
10	2	100	20

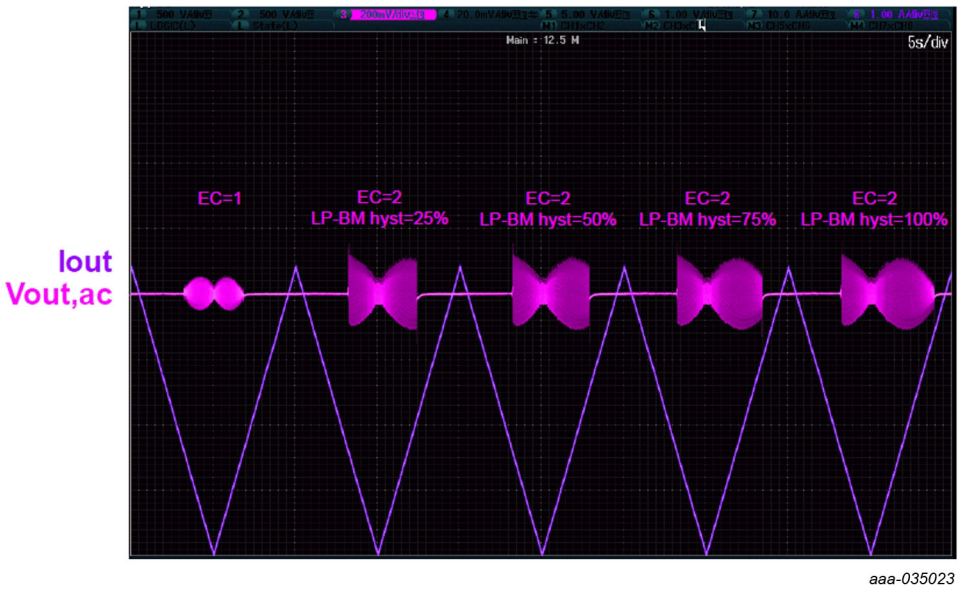


Figure 85. Output voltage ripple at different BM-LP hysteresis values

13.5 Reduce audible noise in burst mode operation

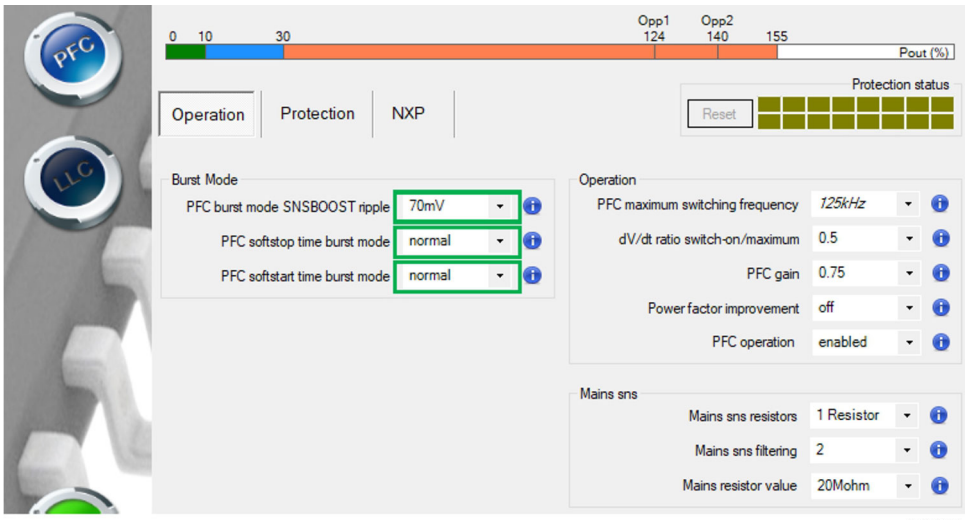


Figure 86. PFC-related parameters that can help to reduce audible noise

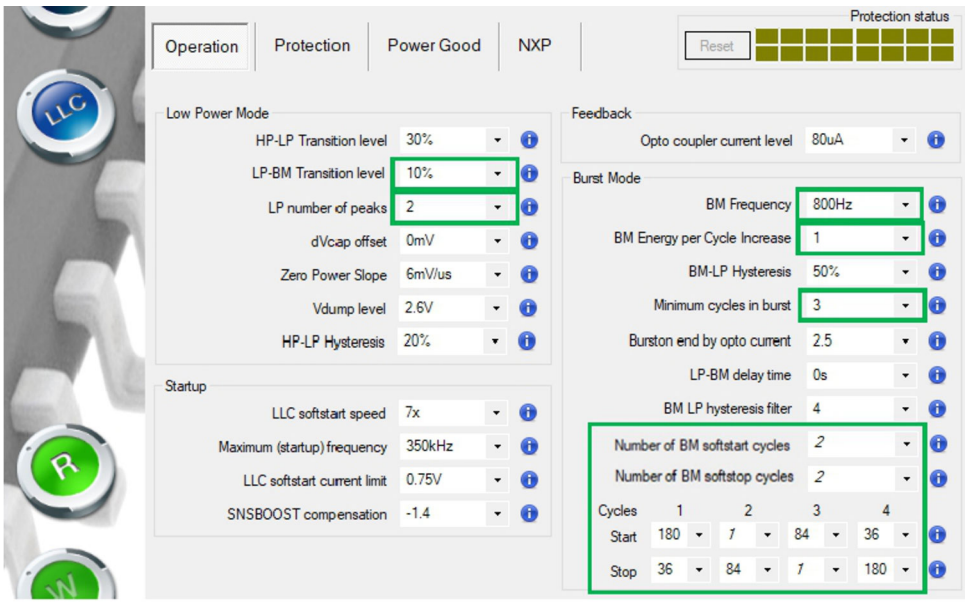


Figure 87. LLC-related parameters that can help to reduce audible noise

13.5.1 PFC audible noise reduction

13.5.1.1 PFC soft start and soft stop time

To reduce the audible noise from the PFC coil, a soft start and/or a soft stop can be added to the PFC burst. These functions can be activated using a setting with a selectable value for the soft start/stop time.

The PFC on-time is increased (soft start) or reduced (soft stop) during the selected time. It avoids a repetitive significant current step in the PFC coil that can generate audible noise. The selected time value (short, normal, long) is just an indicator during the resulting soft start/stop behavior, because the normal PFC regulation is active during this period and strongly influences the on-time.

Adding soft start and soft stop slightly reduces the efficiency. How much the efficiency changes, depends on the load condition and the setting for SNSBOOST ripple.

13.5.1.2 PFC burst mode SNSBOOST ripple

The setting for SNSBOOST ripple can influence the audible noise behavior of the LLC converter by the variation of the V_{boost} voltage during PFC burst mode operation.

The PFC can operate in two types of burst mode. The type can be selected using the PFC burst mode SNSBOOST ripple setting.

Figure 88 shows the two types of PFC burst mode the behavior of the PFC in burst mode.

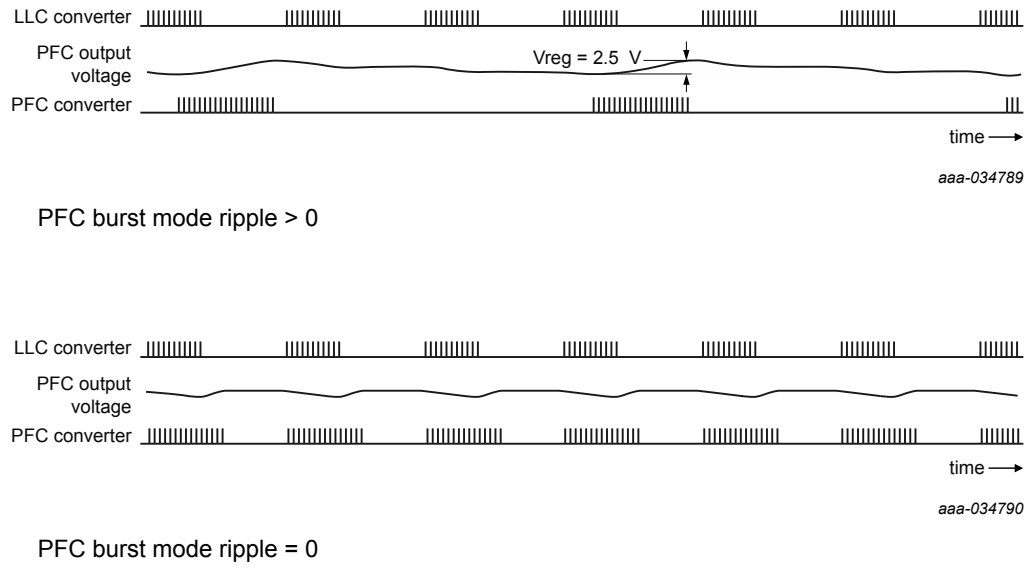


Figure 88. PFC burst mode by output voltage ripple or synchronous with LLC burst

The best setting for audible noise depends on the measurement conditions. It can vary for different output loads. Practical measurements and trials, including requirements for efficiency, can show the best choice.

13.5.2 LLC audible noise reduction

The burst mode switching consists of LP cycles. Also, for audible noise in BM, the LP repetition frequency must be set above the audible frequency range.

The TEA2016AAT offers four parameters that directly help to reduce audible noise for LLC burst mode operation.

- LP number of peaks: a lower number of peaks increases the LP repetition frequency to above 20 kHz with margin.
- BM repetition frequency: a lower repetition frequency reduces the audible noise. The output voltage requirements limit this setting, because it also increases the output voltage ripple.
- LLC burst mode number of soft start cycles. The use of BM soft start reduces the audible noise of the LLC transformer by avoiding a repetitive large initial current step.
- LLC burst mode number of soft stop cycles. The use of BM soft stop reduces the audible noise of the LLC transformer by avoiding a repetitive large current step at the end of each burst.

In addition, the power range for burst mode operation can set the LP-BM transition level. Limit the BM power range to what is necessary to meet design specs.

The BM energy-per-cycle increase is intended to increase efficiency. But at the lowest load conditions, it reduces the repetition frequency. So, it also helps to reduce audible noise.

13.5.2.1 LLC soft start and soft stop basic

Basic use of this function already provides a good improvement on audible noise. The basic setting only makes the first and the last current pulse of the burst small.

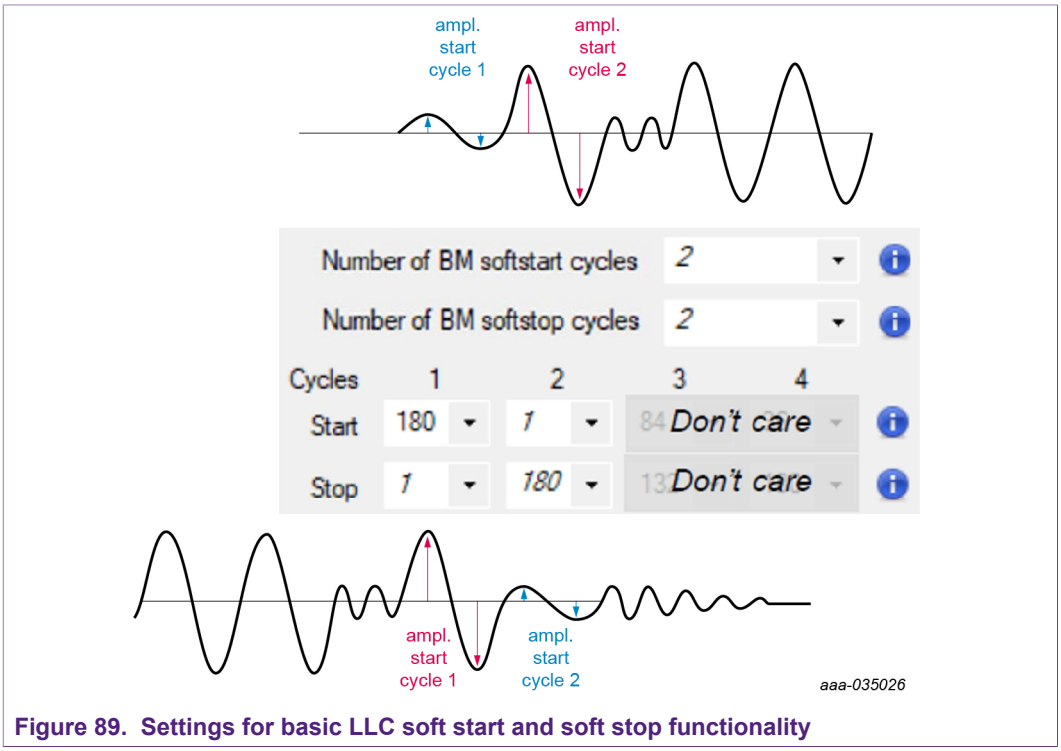


Figure 89. Settings for basic LLC soft start and soft stop functionality

This way of using the LLC soft start and soft stop function works well in most applications.

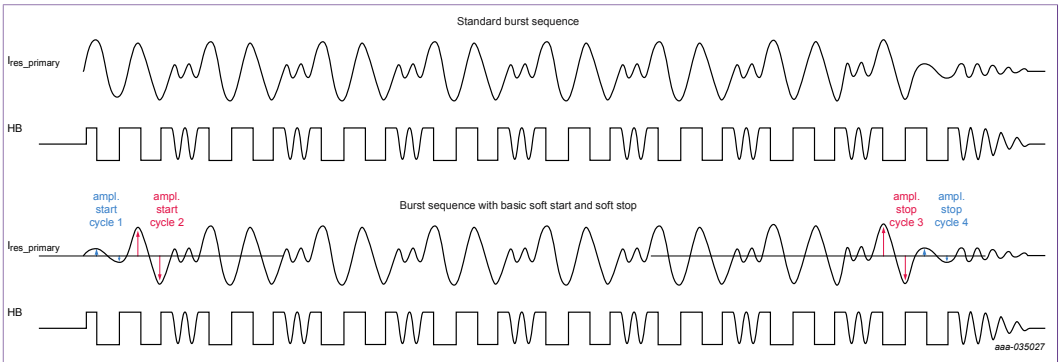


Figure 90. Settings for basic LLC soft start and soft stop functionality - timing diagram

13.5.2.2 LLC soft start and soft stop advanced

Selecting settings on four cycles can optimize the soft start and the soft stop function. The behavior depends on the application conditions. A change in other BM energy-per-cycle related parameter settings or related system component values, changes the soft start and soft stop behavior. In practice, optimization is required. It is good to recheck the function after all other design work is finished.

When optimizing the settings it is important to measure the audible noise results. Normally, a gradual increase and decrease of the resonant current amplitude provides the best result.

A setting of 1 cycle can influence the results of an adjacent cycle because of the dynamic system behavior. After some iterations, a best result can be found.

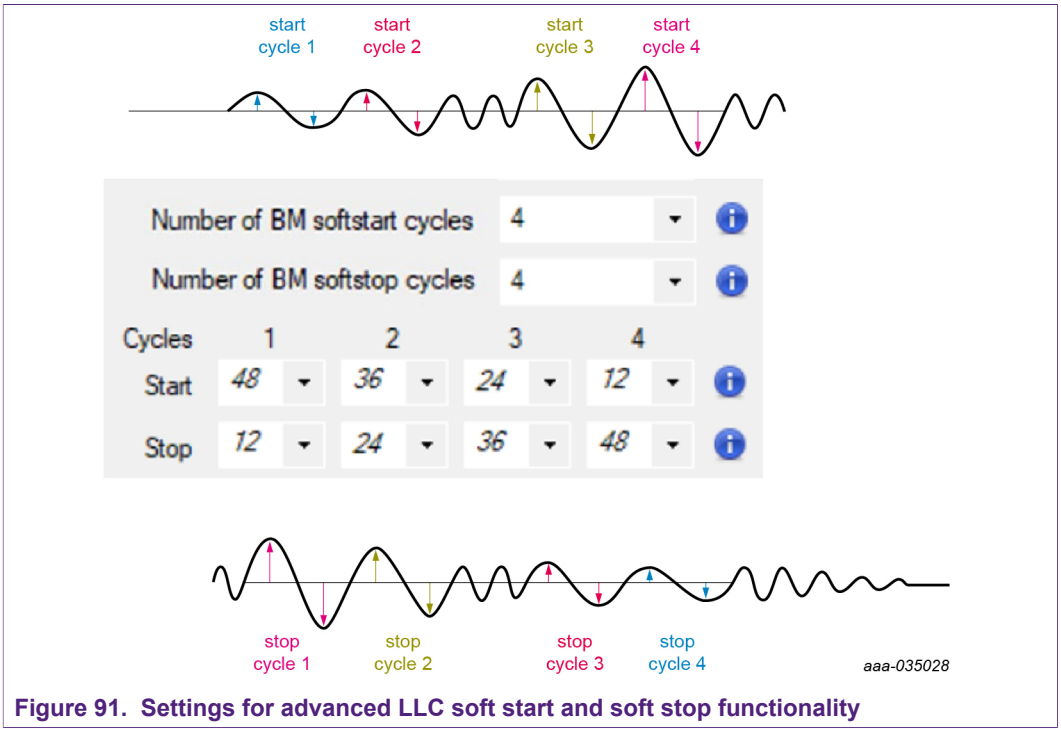


Figure 91. Settings for advanced LLC soft start and soft stop functionality

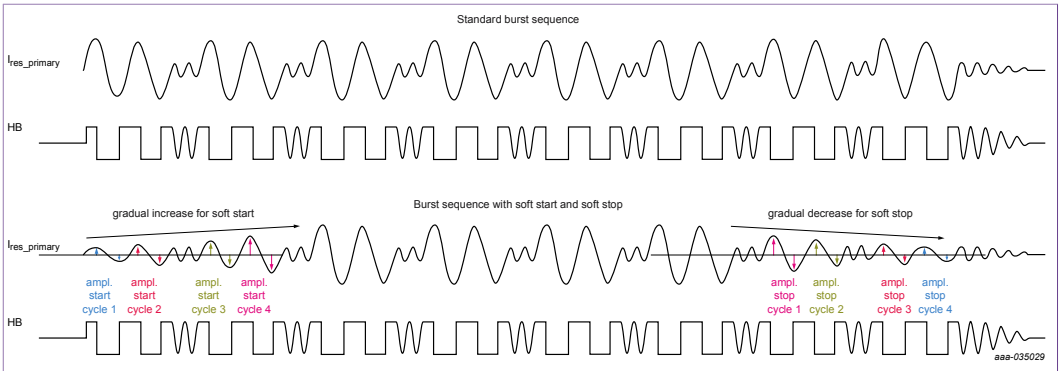


Figure 92. Settings for advanced LLC soft start and soft stop functionality

13.5.2.3 LLC soft start and soft stop adds switching cycles

Using the LLC soft start and soft stop function adds extra cycles to a burst. It has a small negative effect on efficiency because the amplitude reduction in the soft start and the soft stop cycles also reduces the output current. This efficiency reduction is usually very small.

Using the basic setting ensures minimum loss of efficiency while still providing a good reduction of audible noise.

13.5.2.4 LLC soft start and soft stop disabled

Selecting zero number of cycles for LLC BM soft start and LLC BM soft stop disables this function. No extra cycles are added to the burst.

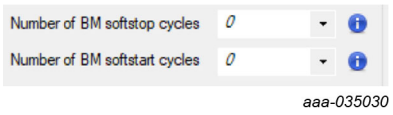


Figure 93. Disable LLC soft start and soft stop functionality

13.6 Reduce output voltage ripple

13.6.1 Reducing output voltage ripple in Burst Mode (BM) operation

See Section 13.4.

13.6.2 Reducing output voltage ripple in low-power (LP) mode operation

Normally, the highest output voltage ripple is found in BM at 50 % LLC burst duty cycle or in HP full-load operation.

In LP, the maximum output voltage ripple is found at the highest power level within LP operation. In the transition from HP to LP, the energy-per-cycle is increased to compensate for the time.

A lower HP-LP transition level reduces the maximum output voltage ripple in LP mode.

13.6.3 Reducing output voltage ripple in High Power (HP) mode operation

Reducing the output voltage ripple can be done using external components on the output. An extra LC filter on the output can effectively reduce the LLC switching frequency ripple.

A disturbance of PFC switching in the feedback loop near the output error amplifier can cause a mains voltage-related ripple. Careful PCB layout can prevent this disturbance (see Section 14.1 and Section 14.2). Increasing the setting for the optocoupler current level can reduce the sensitivity for disturbance. However, it also results in a higher power consumption that has a significant effect on the efficiency in low-load operation.

13.7 PFC Start-up

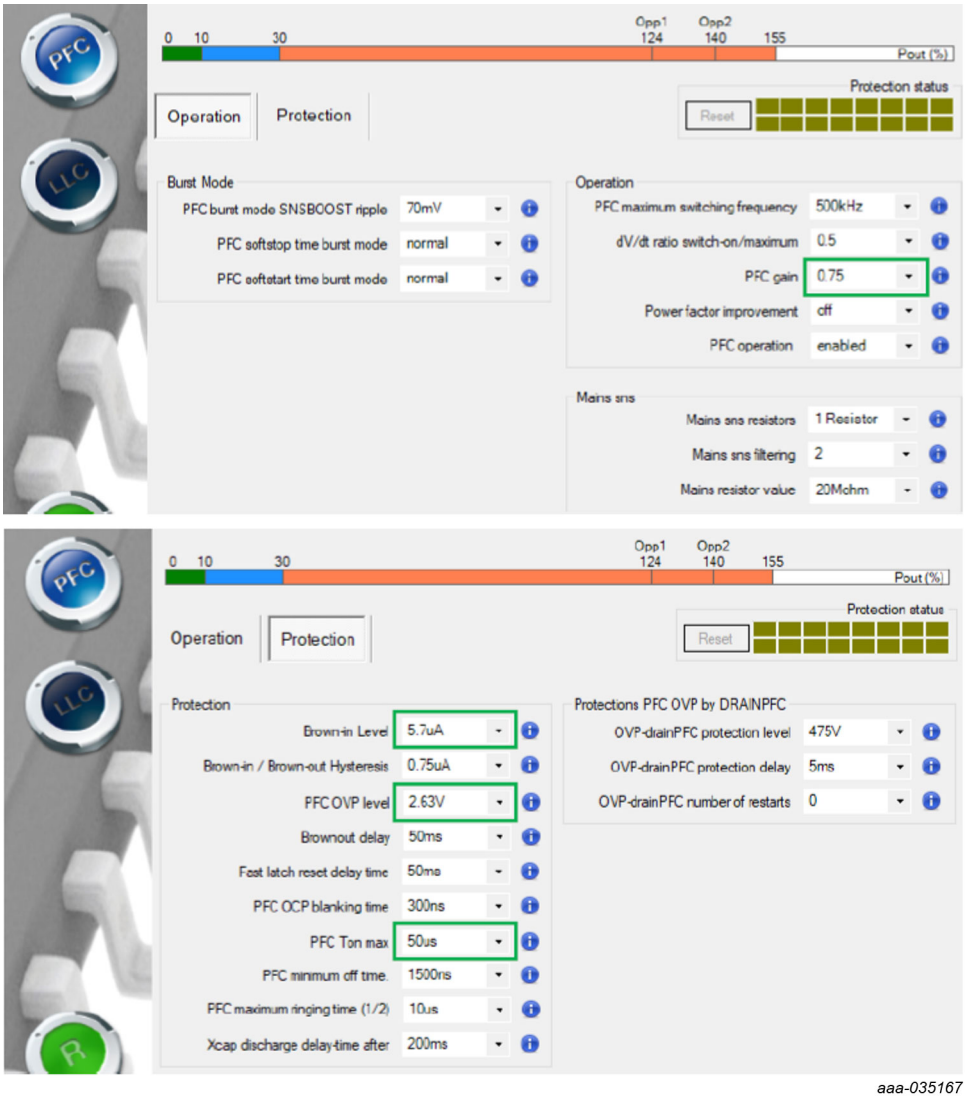


Figure 94. Parameter settings that influence PFC start-up

13.7.1 PFC mains brownin level

With this parameter, the lowest mains value for start-up is defined (see Section 8.3).

When starting at a higher mains voltage, the brownin level setting does not change the PFC start-up behavior.

13.7.2 PFC start-up time

The PFC $t_{on(max)}$ setting and the PFC gain setting influence the time duration from start-up until the nominal output voltage is reached. Both affect the start-up speed. At a higher setting value, the start-up time duration is shorter.

13.7.3 V_{boost} overshoot

At lower LLC load conditions during start-up, the PFC output voltage, V_{boost}, can show a voltage overshoot. The resulting behavior depends on the PFC components, the load condition, and the following parameter settings:

- PFC gain
- PFC $t_{on(max)}$
- PFC OVP level

When the PFC OVP level is triggered, PFC switching is temporarily interrupted. A higher PFC OVP level value and reducing the PFC output voltage overshoot reduces the chance of such an interruption.

A lower value for the PFC gain and PFC $t_{on(max)}$ can reduce a PFC output voltage overshoot.

To protect the V_{boost} output capacitor or regulate the performance at load steps or mains interruptions, the three parameters are chosen for best performance during normal operation. However, they also influence the start-up behavior. In some cases, for the best setting, a trade-off is necessary.

13.8 LLC start-up

13.8.1 SNSBOOST LLC brownin level

When the input voltage (V_{boost}) is close to the nominal value, the LLC converter can start. SNSBOOST senses the LLC input voltage and the start voltage level can be selected using a parameter setting.

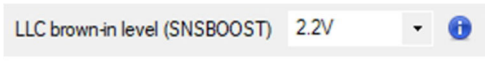


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Figure 95. SNSBOOST LLC start level

Because the LLC converter starts when the PFC start-up is not yet completed, the converters influence each other during this period. A higher LLC brownin level value reduces this period. To decide what the best value is for an application, practical measurements can help.

13.8.2 LLC output voltage increase and primary current amplitude

To determine what the best start-up settings are, the primary LLC current amplitude and the LLC output voltage increase can be observed. It is important to observe the

primary LLC current amplitude and the LLC output voltage increase at a few different load conditions because they significantly influence the behavior.

To optimize the behavior, three parameters can be used:

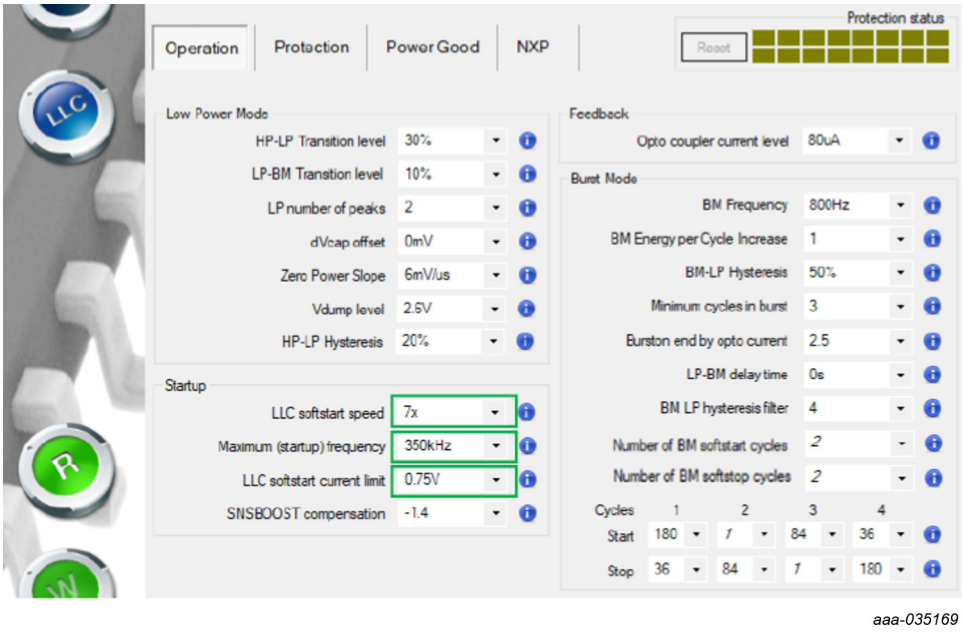


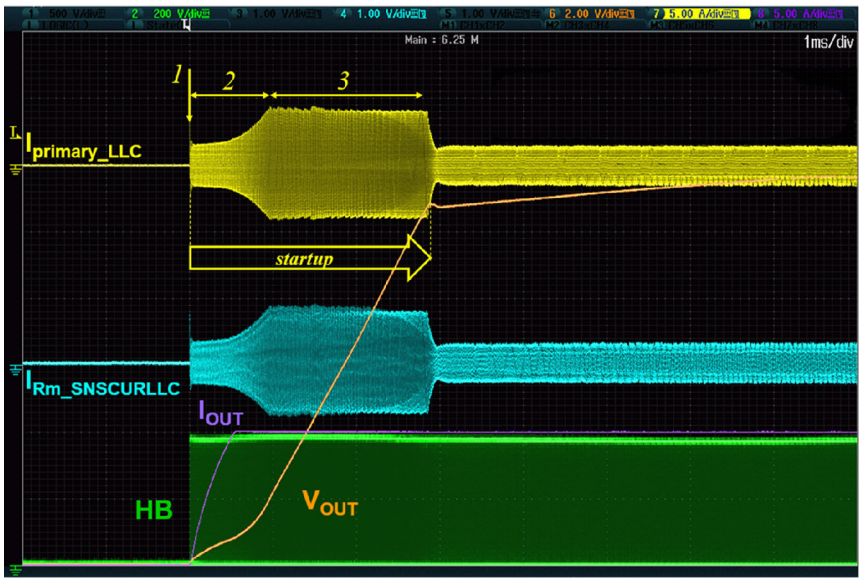
Figure 96. Parameter settings that influence LLC start-up

The LLC starts up with a soft start that limits the primary current amplitude. The SNSCURLLC voltage represents the primary current value.

- The maximum (start-up) frequency limits the current during the first switching cycles by starting the switching at a (selectable) high frequency.
- The LLC soft-start current limit limits the primary current amplitude during the complete start-up period. Usually, near the end of the start-up, the current is constantly limited.
- The LLC soft-start speed setting changes the intended duration of the soft start period. However, the current limiting function has a higher priority and can delay the start-up progress significantly.

Figure 97 shows 3 steps in the LLC start-up that can be modified using the parameter settings

Figure 98 shows 3 examples of resulting behavior when changing one of the 3 parameter values.



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1. First switching cycles
2. Current and voltage increase
3. Current limit

Figure 97. LLC start-up in 3 steps

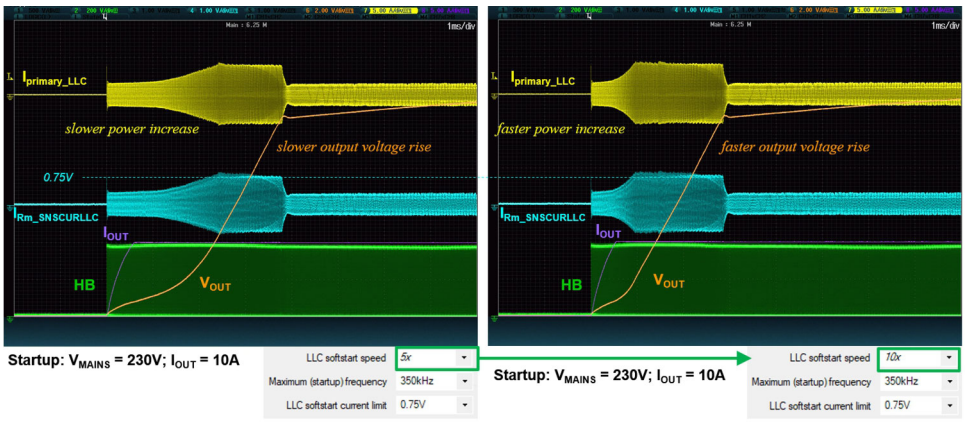

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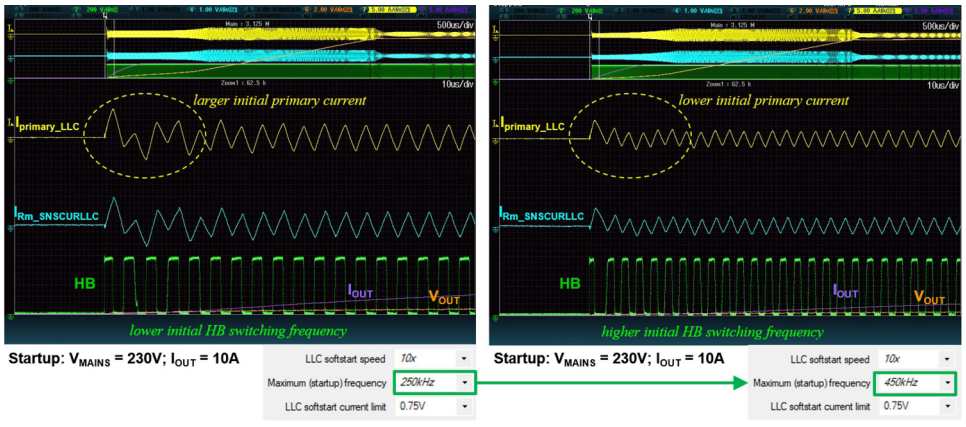
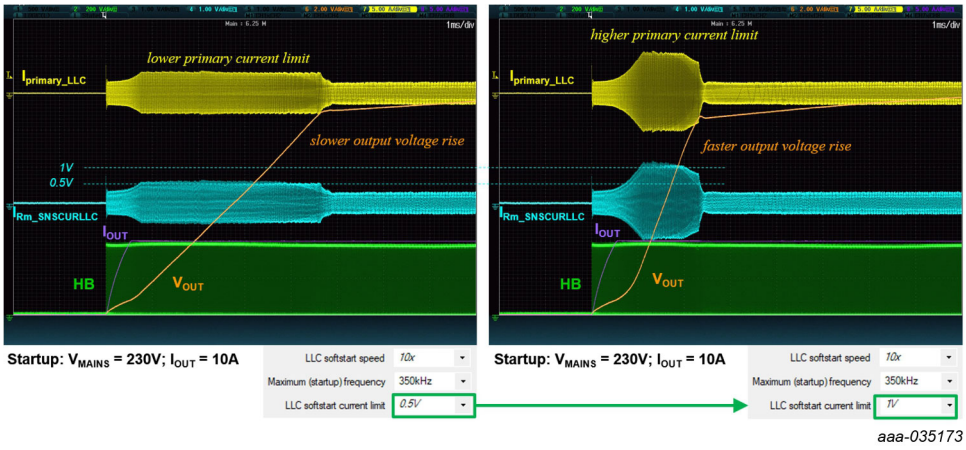
Figure 98. Examples of changed start-up behavior by different setting values





In many cases, the default settings result in a good start-up behavior. In some cases, where performance requirements are stricter or the application design is special, to obtain the best result, modification is necessary.

The LLC soft-start current limit is the same function as the OCP function during normal operation. But the limiting levels are lower and only valid during start-up. In several power supply designs, like in TEA2016DB1519v2, the OCP is only used during start-up. In most cases, the OPP and power limit function limit and protect during overload or output short-circuit conditions at normal operation. During normal operation, the OCP is only triggered sometimes as a temporary “emergency break” limiter. To obtain the best balance between the start-up current limit and the OCP functionality during operation, the SNSCURLL circuit design and the start-up parameter settings can be optimized.

The setting for maximum (start-up) frequency is not only intended for start-up, but it is a general maximum frequency selection. It is similar to setting the maximum frequency in a frequency controlled LLC system.

13.8.3 Current limiting during LLC start-up

When the voltage on the SNSCURLLC pin exceeds the selected limit level, the progress of the soft-start sweep is temporarily put on hold. When $V_{SNSCURLLC}$ drops to below the current limit level again, the soft-start sweep continues.

In addition to the output voltage increase and the switching timing, V_{BOOST} and the related SNSBOOST compensation can influence the amplitude of the primary current.

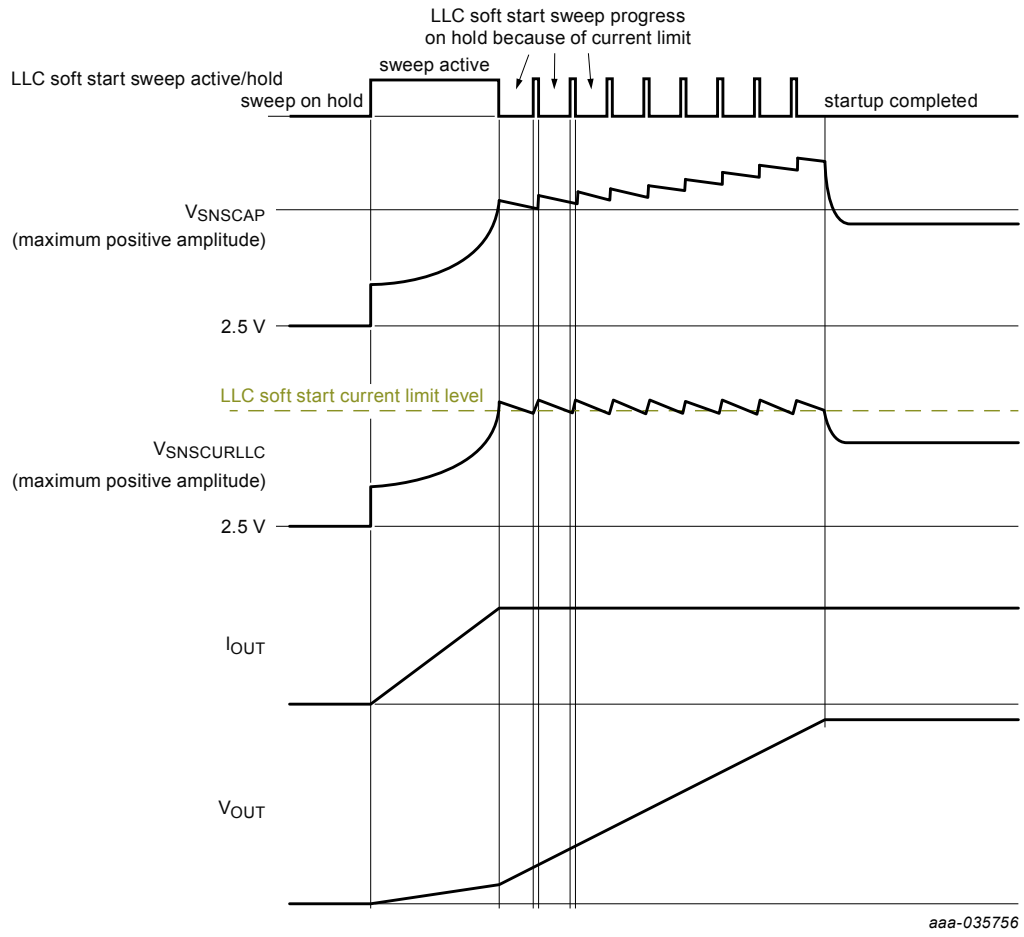


Figure 99. Current limit SNSCURLLC during start-up

13.8.4 Maximum start-up time protection

Usually, the LLC start-up only takes several milliseconds (see examples in Figure 98). If a defect or an overload condition occurs, the maximum start-up time protection can be triggered after the preset time. The resulting protection behavior follows the settings for OPP: safe restart, restart time, latched, etc.

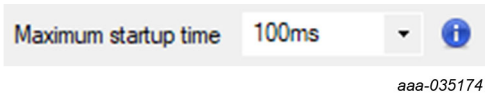


Figure 100. Maximum start-up time protection

When SNSFB current starts flowing, the system assumes that the start-up is finished. Normally, when the LLC output voltage is close to the regulation level, a secondary error amplifier starts to pull current.

13.9 Power good

For housekeeping of the total system, a power good signal can be used to communicate a basic message to the application that is supplied by the power supply.

- Power delivery is stable after start-up; power supply is OK
- Power delivery goes down (soon); power supply is (soon) not OK

The TEA2016AAT supports such a function by making the SNSFB output pin voltage high or low, depending on the state of the power supply. The SNSFB pin is also used for LLC feedback regulation by the SNSFB current.

The SNSFB output is made active high after start-up. This condition shows that the converter output voltage is not yet OK because the system is in a start-up condition. The default delay time is 5 ms (see Figure 102)

After start-up, when the system enters the operating state, the SNSFB output is pulled low to show that the SNSFB voltage output is OK.

The combined power good and SNSFB functions are shown in Figure 101.

A pull-up circuit on primary and secondary side, connected by an optocoupler, provides the power good signal to the application that is supplied by the power supply.

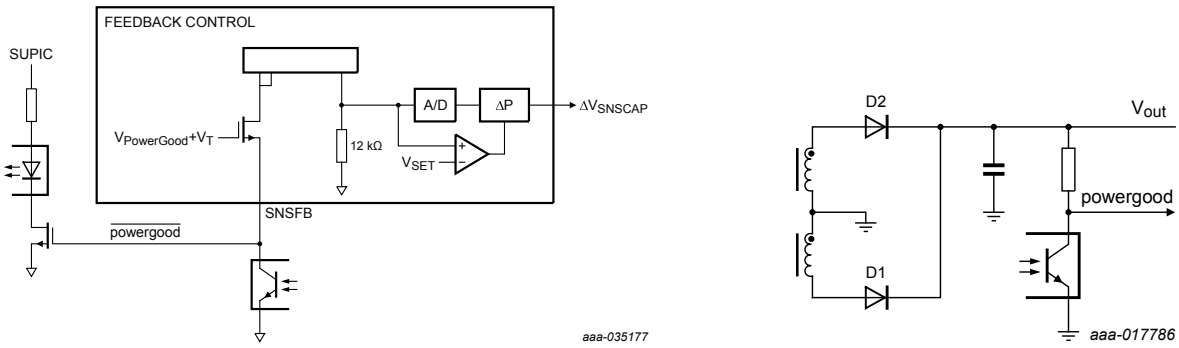


Figure 101. Power good combined on SNSFB

Figure 6 shows the combination of SNSFB current for regulation and the voltage for power good in a timing sequence during start-up, protection, and stop operation.

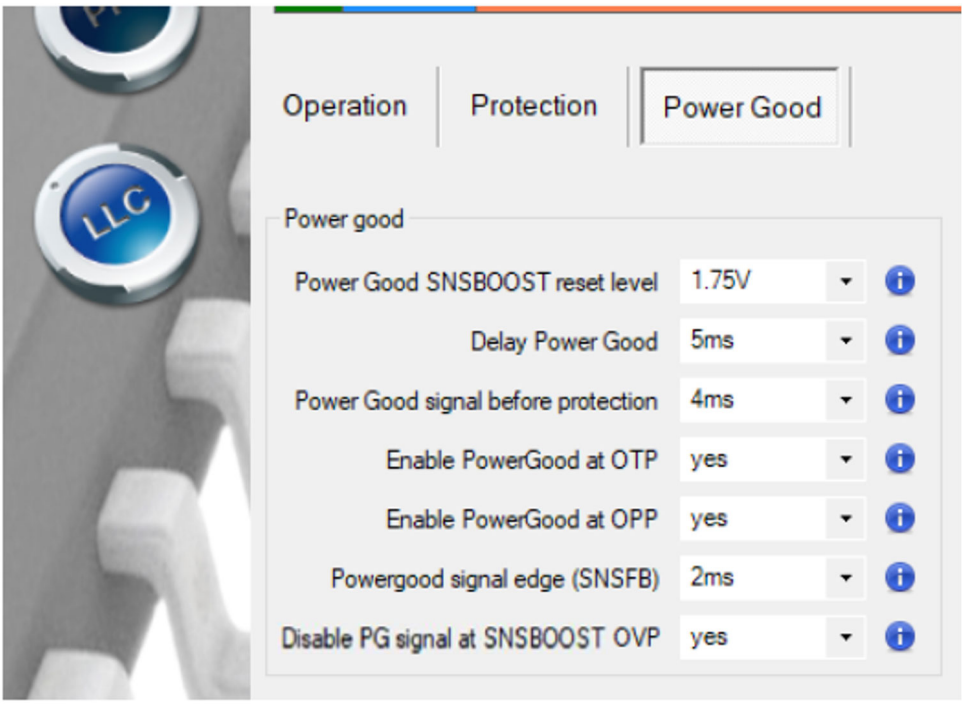


Figure 102. Power good settings

In alignment with the selected option for several parameters, the SNSFB voltage becomes active high when:

- The voltage on the SNSBOOST pin drops to below 1.75 V (default value)
- The OPP counter is close to its end value (default is yes; default is 4 ms in advance)
- The converter is about to stop due to an OTP protection (default is yes; default is 4 ms in advance)
- When the system enters the protection mode (OVP, OCP, or UVP), it pulls high the SNSFB pin and stops switching immediately.

To avoid any disturbance of the regulation loop (SNSFB current), the increase and decrease of the SNSFB voltage is in alignment with a predefined ramp (default setting is 2 ms). The options for different values are intended to optimize the transition of the resulting power good signal on the secondary side.

The best choice of settings for the power good parameters mainly depends on system requirements from the application that is powered by the power supply.

13.10 Mains sensing

The mains voltage value measured by SNSMAINS is used to start and stop the PFC converter but also to compensate the PFC feedback loop. The mains sensing function uses an internal analog-to-digital (AD) conversion with a resolution of approximately 3 V.

When the mains sensing current is disturbed or unstable, the measurement result can vary in time if it is close to a transition of the 3 V intervals. It can lead to a series of small loop corrections in the course of time.

The mains SNS filtering parameter function can help to filter these variations to a stable reading.

Figure 103. Mains SNS filtering parameter function

When the SNSMAINS disturbance or variations occur often, a higher filter value can be chosen to filter over a longer time. The filter value represents the number of measurements over which the resulting value is averaged.

The number of mains measurements in time depends on the use of one measurement resistor (one measurement during a mains period) or two measurement resistors (two measurements during a mains period). It also depends on the mains period time (frequency) itself.

A disadvantage of using a high filter value is that the reaction to a normal change in mains voltage is slower.

Careful PCB design (see Section 14.6) can minimize disturbances on the mains measurement.

In some cases, the use of an extra analog filter can be considered. The filter must not give too much distortion of the mains sine wave signal but suppress higher frequency disturbances.

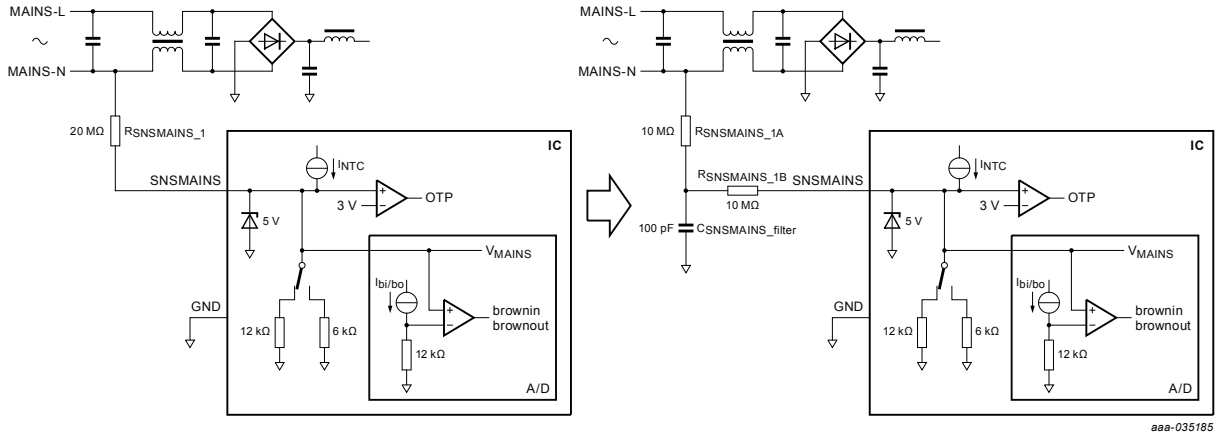


Figure 104. Example of an extra SNSMAINS filter for 50 Hz/60 Hz applications

13.11 Power factor improvement

The PFC converter and the mains input design basically determine the power factor performance of a power supply.

However, the TEA2016AAT offers two functions that can provide a small additional improvement.

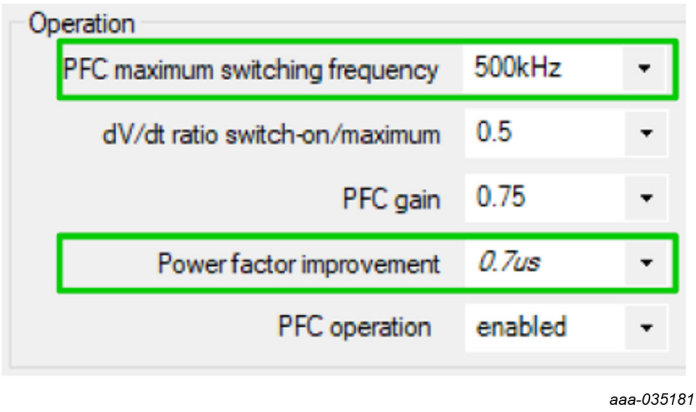


Figure 105. PFC frequency limit and power factor improvement function

Section 16.4 and Section 16.5.3 give a description of the functions.

Both functions help to gain performance on the power factor value in the medium power range at high mains voltage.

Practical measurements with different settings can directly show the result on improvement. It is important is to check for a possible reduction in efficiency. In some cases, a compromise in settings is necessary.

A higher maximum PFC switching frequency can improve the PF and THD performance. However, it reduces the efficiency in some load conditions.

The use of the power factor improvement function usually has an improvement on power factor without significant loss in efficiency. In some cases, it can even improve the efficiency. The best value must be found by way of practical experimenting at different load conditions.

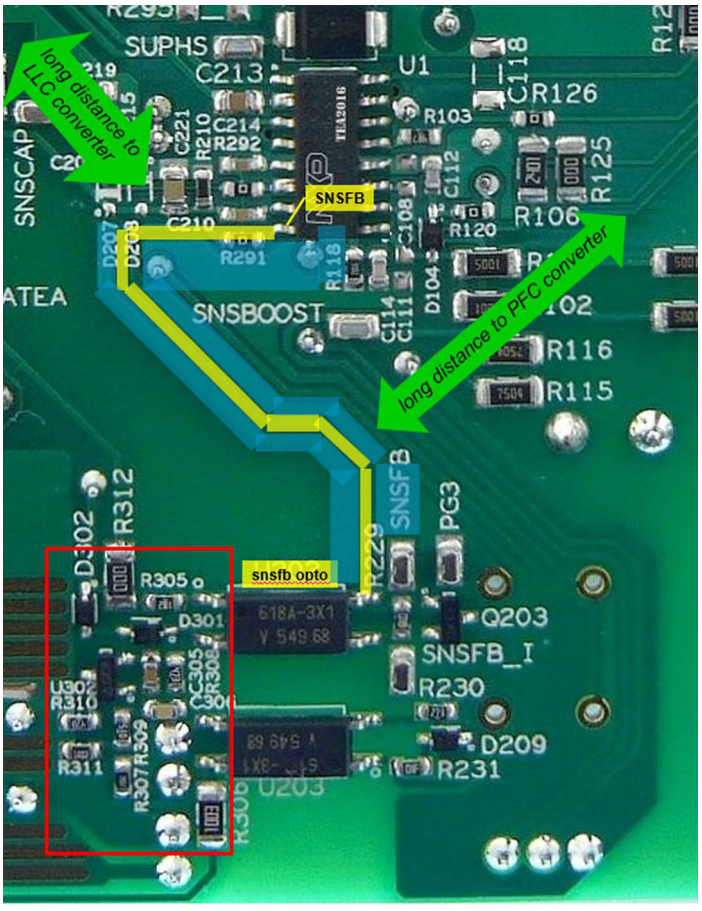
14 Important PCB layout design rules

14.1 SNSFB track shielded by GND tracks/plane

Because the SNSFB function works on low current levels to minimize energy consumption at no load, this signal is more sensitive to disturbance.

Disturbance by capacitive coupling to converter switching tracks (HB or DRAINPFC) can make regulation unstable. To avoid disturbance in SNSFB:

- The SNSFB track must be placed at a relative large distance from the power part of the converters (LLC and PFC).
- Tracks along the SNSFB track must be grounded for shielding (and a ground plane if the design is a double-sided copper design)
- The SNSFB track does not have to be short. To obtain a large distance to HB, a longer track is necessary.



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Yellow marked area: SNSFB
Blue marked area: Shielding GND
Green arrows: showing large distance SNSFB to LLC and PFC converter switching
Red marked area: Shows a compact TL431 circuit design

Figure 106. SNSFB: longer but shielded track with large distance to converter switching

14.2 TL431 circuit must be compact

Because the SNSFB function works on low current levels to minimize energy consumption at no load, the signal is more sensitive to disturbance.

In addition to the SNSFB connection (discussed in Section 14.1), the secondary part of the feedback circuit also operates on a low current. To prevent that PFC switching noise causes a disturbance, it must be made compact in size. This type of disturbance leads to extra output voltage ripple of 100 Hz or 120 Hz and is mains voltage related.

14.3 Separate GND connections for LLC and PFC

To avoid mutual disturbances, the grounding of the PFC and LLC controller must be separated in the PCB layout structure. Current pulses through ground tracks can lead to a wrong (voltage) value or a signal on a pin that uses the ground level as a reference.

The main potential sources of disturbance are the significant energy switching of the PFC and LLC converters and the MOSFET gate drive currents generated by the controllers.

Figure 107 shows these energy flows. It also shows that, to avoid disturbances, a special ground structure can keep them separated.

Keep these energy flow loops for each converter as small as possible, concerning track length and surface area.

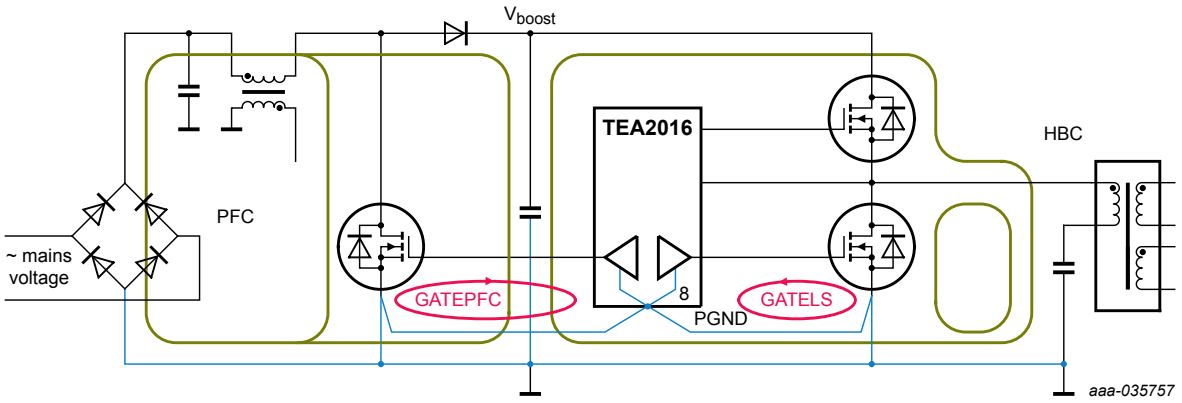


Figure 107. Converter and gate drive currents must be kept in separate tracks

By connecting the IC to the shared bulk capacitor function via a separate ground track, disturbances caused by converter current can be minimized.

14.4 Short track on SNSCURLLC pin

The SNSCURLLC function senses the input signal cycle-by-cycle at low voltage levels with a high impedance input. The signal is applied to the pin with a decoupling capacitor that must be placed very close to the IC to avoid disturbance pickup on the connecting track.

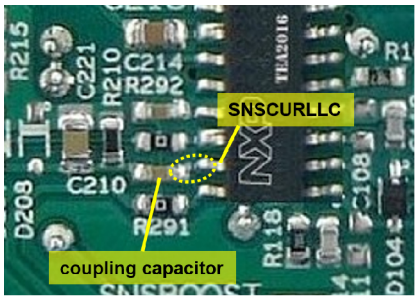


Figure 108. Very short track for the SNSCURLLC pin connection

14.5 GND of V_{cap} divider to SNSCAP must be connected to IC GND

High LLC converter current in the ground connection of the SNSCAP divider can disturb operation and show switching errors. It can be avoided by connecting the GND of the SNSCAP divider to the IC GND and not to the converter GND (C_r).

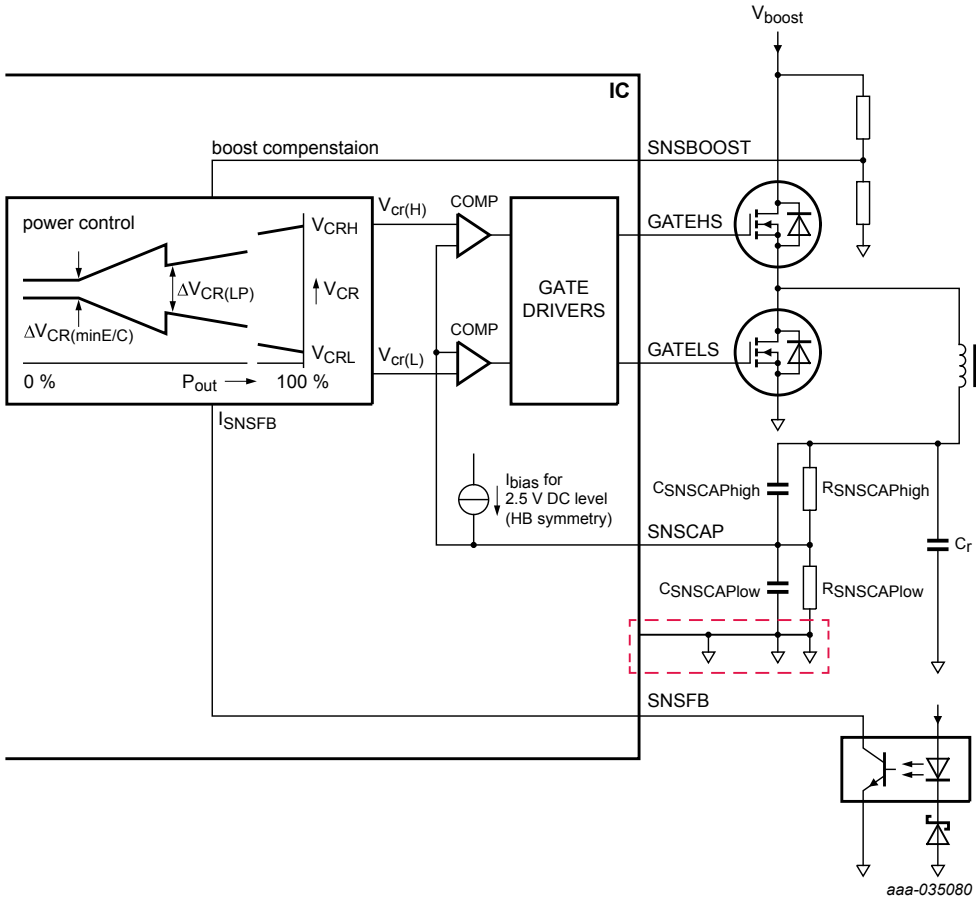


Figure 109. GND of V_{cap} divider to SNSCAP must be connected to IC-GND

14.6 SNSMAINS mains sensing resistors close to IC

To save power, the SNSMAINS mains sensing function of the TEA2016AAT controller uses low current levels. To avoid disturbance, the mains sensing resistors must be placed close to the IC.

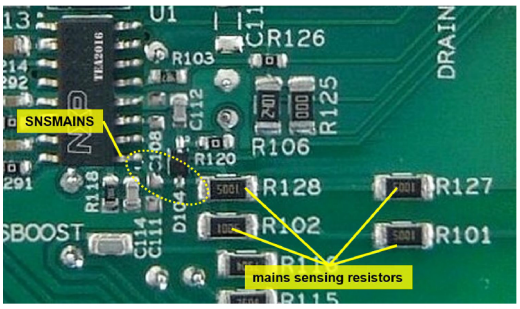


Figure 110. SNSMAINS mains sensing resistors close to the IC

14.7 I^2C connection tracks on HV spacer pins

To avoid that HB pulses disturb the communication for development purposes, place the I^2C tracks as far away from the HB tracks (HB, SUPHS, and GATEHS) as possible. The distance from the I^2C tracks to the track connected to DRAINPFC must also be as large as possible.

It is impossible to keep the distance large close to the IC. However, it can be done along the rest of the tracks.

15 Programming internal settings

15.1 MTP memory and registers

The MTP in the IC is a permanent (but changeable) memory like a flash memory. When the IC supply voltage goes down, the content remains.

The registers in the IC are a temporary memory. When the supply voltage goes down, the content is lost.

15.1.1 IC operation

For correct operation, the stored MTP setting values are copied to the registers at start-up.

The IC operation works with the register values. It can only store the protection registers in the MTP memory. The user or a programming unit must store the remaining MTP content.

15.1.2 Default settings

When erasing the MTP (setting all values to zero), the settings are at default. The default values show a predefined “middle of the road” type of operation. Most applications run well but not optimal at default values. In some cases, the default settings conflict with the values of the converter and external component values which can lead to the triggering of a protection.

15.1.3 Changing settings

The user can read and write the MTP and the registers via I^2C. A TEA2016AAT-specific I^2C-based protocol is required.

Settings can be changed individually. A complete collection of settings can be saved on the computer as a .mif file. A saved .mif file can be used to program the MTP of an IC.

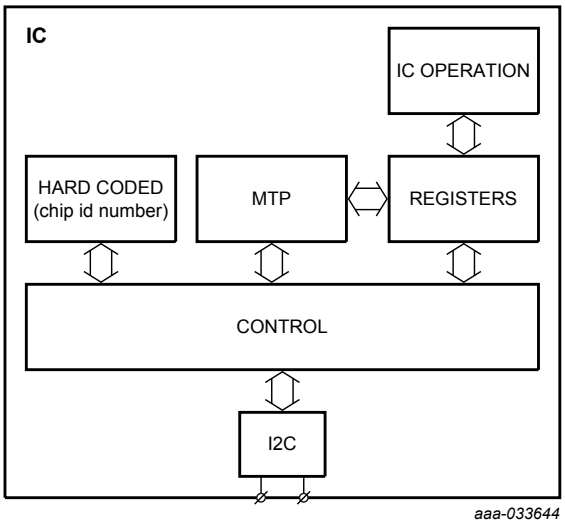


Figure 111. Communication channels with MTP and registers

15.2 Protection registers

The protection registers status are read at start-up. If a protection is triggered, it is set in the MTP, unless it was already set before. Setting the protection in the MTP avoids unnecessary MTP writing.

Table 10. Protection registers list (in order of export settings)

	Protection
1	PFC overcurrent protection
2	PFC overvoltage protection (DRAINPFC)
3	PFC overvoltage protection (SNSBOOST)
4	LLC OPP1
5	LLC OPP2
6	LLC maximum start-up time exceeded
7	LLC overcurrent protection
8	LLC overvoltage protection
9	External overtemperature protection
10	Internal overtemperature protection
11	Fast disable
12	LLC maximum on-time exceeded
13	LLC maximum optocoupler current in burst mode
14	LLC capacitive mode
15	MTP read failure
16	OPP via SUPIC UVP

If the IC is not locked, the registers can be reset using the GUI.

15.3 I^2C communication

In addition to the normal TEA2016AAT ICs, NXP Semiconductors provide special IC versions for product development. The development IC samples provide a second I^2C interface for easy modification of settings while the IC is operating. So the operation can be changed “on the fly”.

15.3.1 Development IC samples: SDA and SCL on spacer pins

Connections to the second I^2C interface of the IC are provided on the pins that are normally not connected, high-voltage spacer pins 7 and 12.

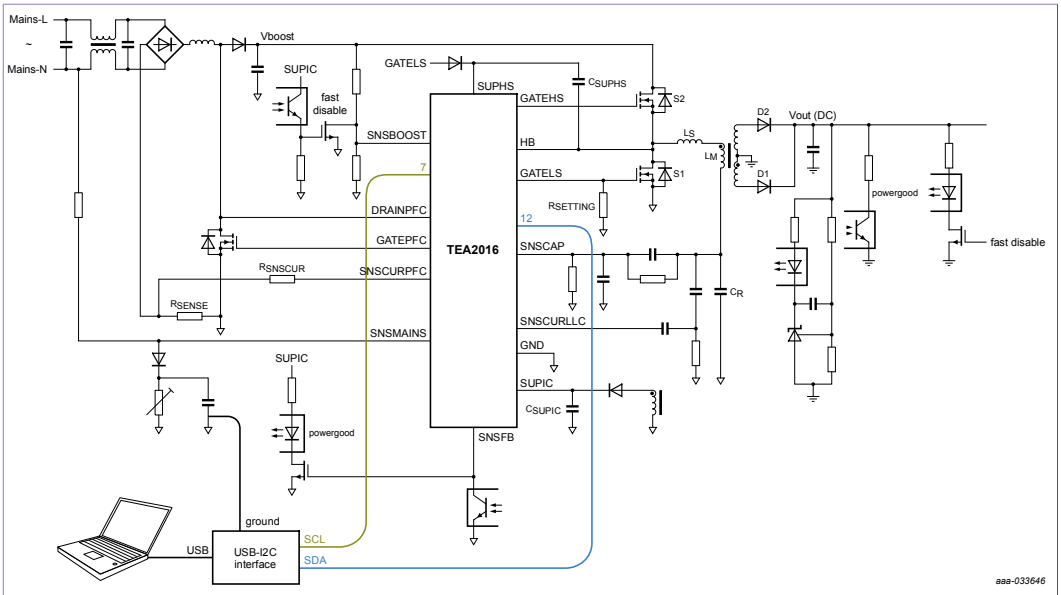


Figure 112. Development IC: I²C connections with spacer pins

The basic I²C interface functions on the combined function pins in the IC are also available on development samples.

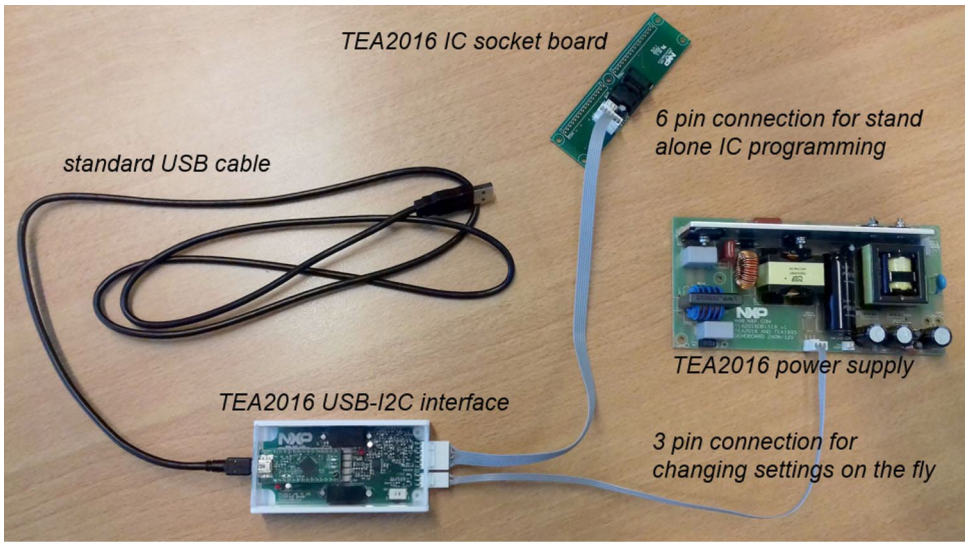


Figure 113. Two TEA2016AAT programming setups: on-the-fly and standalone

15.3.2 Production IC samples: SDA and SCL on combined pins

The basic I²C interface in the IC is available on the combined pins SNSCURPFC (SCL) and SNSCAP (SDA). To program the IC, the IC must be put in the disabled condition pulling SNSBOOST to GND. During programming, SUPIC must supply the IC.

Programming can be done on a separate IC (put in an IC socket) or when the IC is mounted on the power supply PCB.

When programming is done while the IC is mounted on the power supply board, the impedance on the SDA and SCL lines becomes much lower. The much lower impedance endangers communication because rise times and fall times of the communication pulses become much slower and distorted. Depending on the application component values, the driver capability of the I^2C interface must be modified to ensure reliable programming.

15.4 Graphical user interface (GUI) and USB-I^2C interface

During power supply development, a GUI program on a computer and a USB-I^2C interface take care of the communication. The TEA2016AAT GUI provides the correct protocol and offers several options and tools to work with the IC settings.

The TEA2016AAT GUI and USB-I^2C interface user manual shows how to work with it.

The MTP parameter settings can be changed using the NXP Semiconductors “Ringo” GUI software. Before any MTP parameters can be changed using the GUI, the terms and conditions in the start-up pop-up screen must be accepted.

15.5 MTP programming of ICs for production

The TEA2016AAT is very suitable for making an ASIC using dedicated best parameter settings for specific types of power supply. The user can make the ASICs by programming settings before production of the power supplies or even when the IC is already mounted on the power supply.

15.5.1 Vendor code

To identify the ASIC, a 16-bit value can be stored in the MTP. This code can always be read, including when the IC is read and write locked.

15.5.2 Read and write lock

To keep the ASIC-specific settings confidential, the IC can be read and write locked. When the IC is locked, the content cannot be read anymore. If necessary, NXP Semiconductors can still read the content for analyses using specific IC production tools.

15.5.3 Reprogram

Programmed ICs can always be reused by resetting them to default values. The reset also unlocks a read and write protection. It helps to reduce stock with obsolete ICs.

TEA2016AAT ICs are provided with standard programming values. Most values are default, providing a good “middle of the road” operation and performance. These ICs are not locked and can be modified.

When programming an ASIC, it may be more convenient to program the complete MTP with the ASIC setting values. An IC can be reprogrammed at least 200 times.

15.5.3.1 Programming ICs

A non-standard I^2C bus sequence is required to start communication with the IC (key function). The remaining communication is similar to the standard I^2C protocol.

On request, an information package for building a production setup is available, including examples. The MTP map in Section 19 shows the location of each setting.

General pin bias conditions for programming:

- SNSBOOST must be connected to GND
- A DC voltage between 20 V and 30 V must be applied on the SUPIC pin (pin 13) and the GND (pin 4)
- SDA is on pin 14 (also used for SNSCAP) and SCL is on pin 3 (also used for SNSCURLLC)

TEA2016AAT SDA and SCL

SDA (pin 14): Fixed voltage levels for detecting high signals (the level must be higher than 1.4 V to be sure) and low signals (the level must be lower than 0.8 V to be sure). Driver for pulling SDA low can sink 6.6 mA or more, including tolerance and temperature.

SCL (pin 3): Fixed voltage levels for detecting high signals (the level must be higher than 1.4 V to be sure) and low signals (the level must be lower than 0.8 V to be sure). It is input only and has no pull down driver.

15.5.3.2 Programming ICs in the application

When a production version IC is already mounted in the power supply, programming or modifying MTP settings requires special attention. The impedance on the I^2C bus is unusually low because of the components (from the power supply design) connected to pin 3 and pin 14. It makes the communication setup critical. Impedance compensation and strong drivers are necessary to make the I^2C pulses reliable for communication.

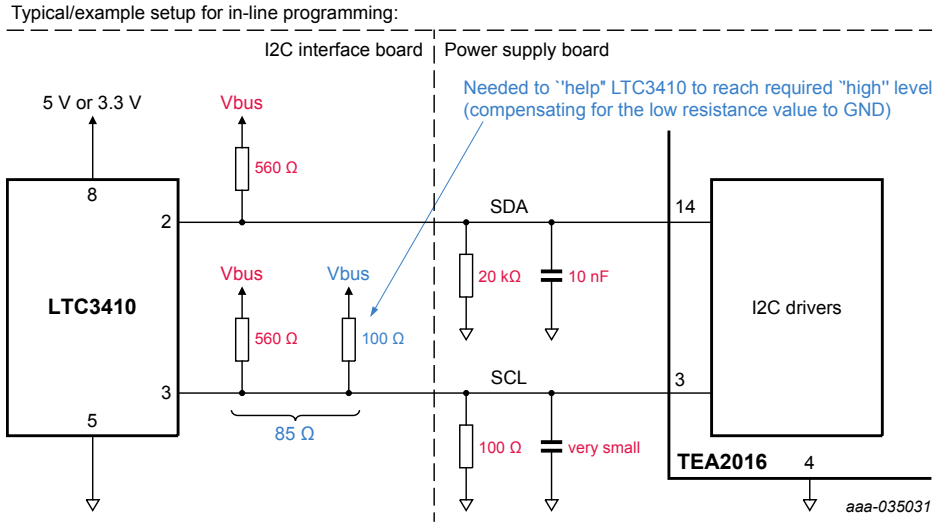
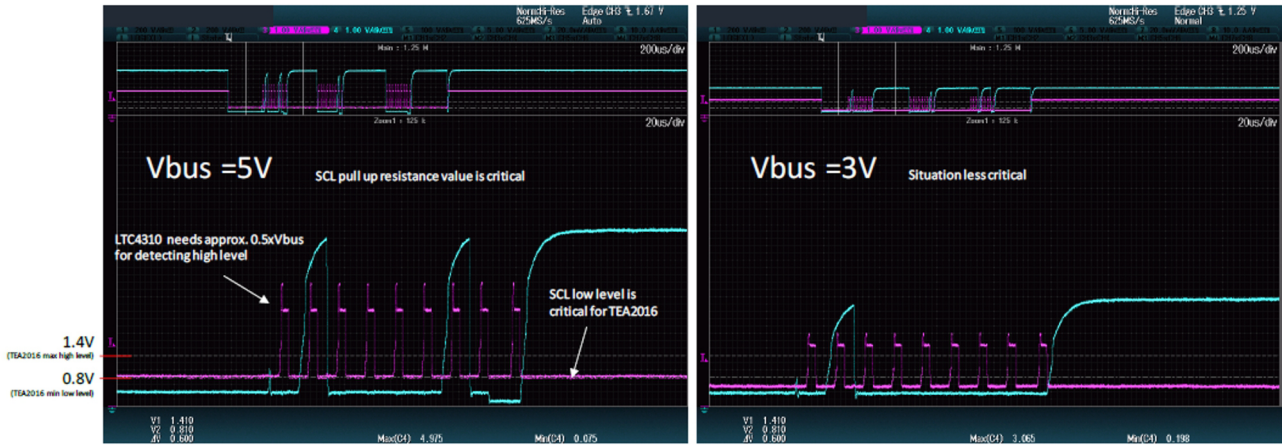


Figure 114. A typical example of compensating the I^2C-bus load by a lower pull-up resistor value



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Communication can still work, but connected components in the power supply severely distort the I^2C signals.

Figure 115. I^2C communication when programming ICs in the application

16 Setting parameters

This section provides information on the settings that are available in the IC.

16.1 Available setting values

The values that are available for a setting are provided by the Ringo software graphical user interface. The displayed values are nominal values.

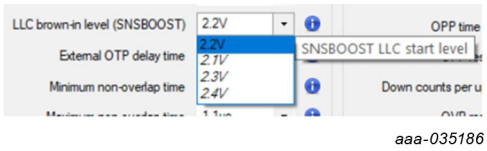


Figure 116. The Ringo GUI provides the available nominal values for a setting

The data sheet provides minimum, typical, and maximum default setting values.

Table 11. Default setting values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{start(SNSBOOST)}$	start voltage on pin SNSBOOST		2.1	2.2	2.3	V

As a rule of thumb, the provided tolerance percentage for the default setting can be used as a tolerance percentage for the other setting values.

16.2 System

16.2.1 SUPIC start level

The SUPIC start level can be selected to be 12 V or 19 V. Typically, when the system uses the integrated HV source for start-up, a level of 19 V must be selected.

When the TEA2016AAT is externally supplied, for instance by a standby supply, the lower start level of 12 V can be used.

16.2.2 Settings for GATELS resistor (R1, R2, R3, R4)

A resistor measurement function in the IC measures the value of the resistor to GND on GATELS. Applying a certain resistor value gives the option to select one of the 4 preselected “menus” each consisting of a group of basic settings related to protections (see Figure 117). It mainly offers a choice between safe restart or latched follow-up character.

Four sets of 8 parameter settings can be chosen. When these sets are programmed, they can be used without reprogramming. Menu R1, Menu R2, Menu R3, and Menu R4 represent the four sets. Figure 117 shows an example of programmed menus.

The 32 fields can be modified independently. However create 4 useful menus that can cover a small variation between applications.

Typically, changing settings with resistor values can be a solution for using the same power supply, changing it from “safe restart” to “latched” using the GATELS resistor

value. It is also possible to use different protection power levels (OCP and OPP) in the menus.

The TEA2016AAT offers a possibility to modify a group of settings with an external resistor value on GATELS without MTP programming.

Other parameter settings do not change with the resistor value.

Figure 117. Overview of settings for 4 different resistor values on GATELS in TEA2016AAT

16.2.3 Maximum start-up time

When the LLC converter starts switching, it expects that the output voltage reaches its regulation level within a maximum start-up time.

To detect the moment that the start-up is completed, the SNSFB current is sensed. When SNSFB current starts flowing, the end of start-up is detected. The allowed start-up time can be set with this parameter. After the time is passed, the system enters a protection mode.

16.3 Mains sensing

16.3.1 Mains sense resistors

The SNSMAINS pin combines two functions:

- The mains voltage sensing
- The sensing of an external NTC for detecting an OTP

The functions are alternatingly active in time.

The measured mains current level is used for the brownout/brownin detection and for the mains compensation in the PFC control loop.

Number of resistors and resistor value

The mains sensing is done by measuring the current through a measurement resistor. There are two options for the measurement resistor.

- Using 1 or 2 measurement resistors.
- The impedance of the resistors is 20 MΩ or 10 MΩ.

When one resistor system is used, the mains peak value is updated every mains cycle. When two resistors are used, the peak value is updated every half mains cycle, allowing a faster reaction to mains value changes.

To realize a low no-load input power level, the external resistor connected to the SNSMAINS pin for measuring the mains input voltage is typically 20 MΩ. Some applications request the lower resistance value of 10 MΩ. The value used can be selected using the mains resistor value setting.

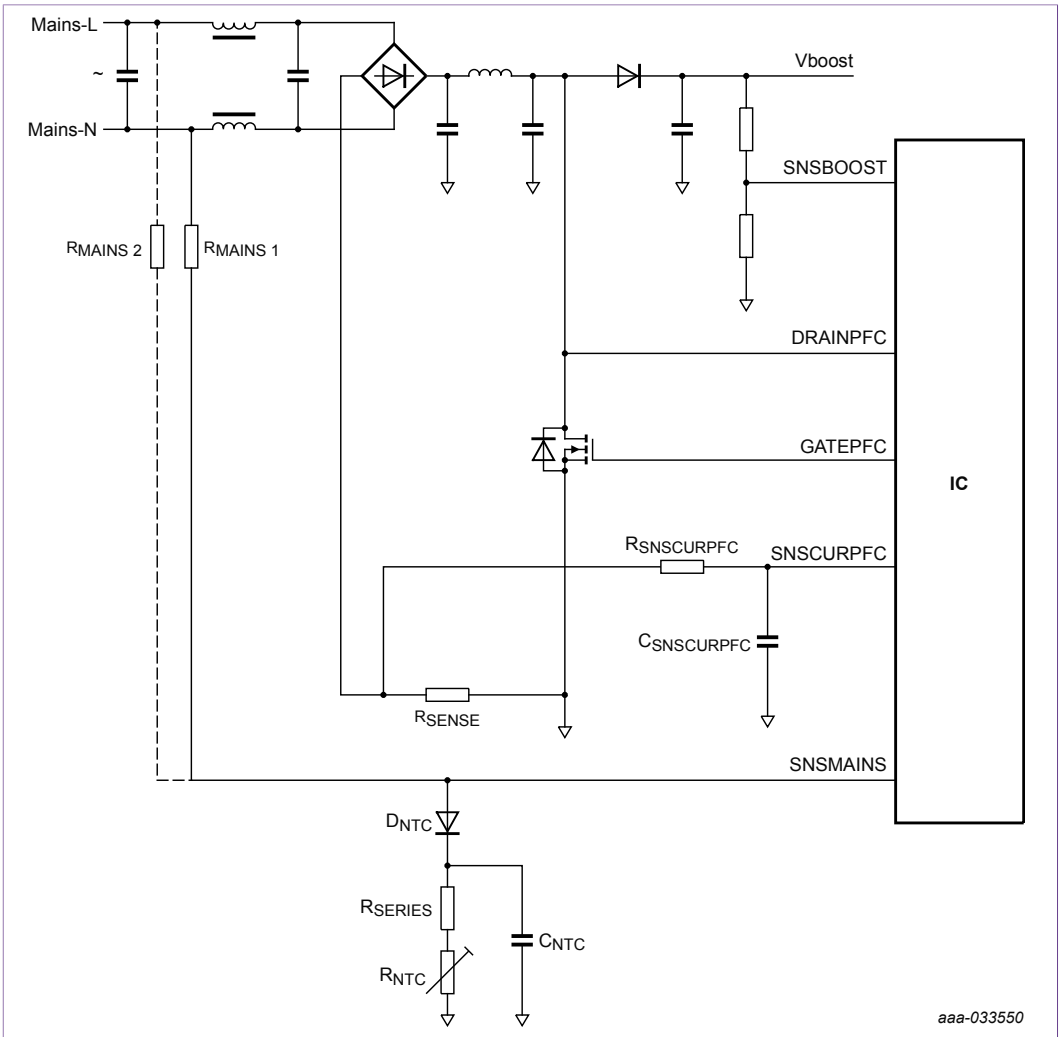


Figure 118. SNSMAINS using 1 or 2 measurement resistors

16.3.2 Mains resistor value

See Section 16.3.1.

16.3.3 Mains sensing filter

The actual mains sensing value is averaged over a number of measurements. The number of measurements that is used for averaging can be selected.

When the 1-resistor system is used, the mains peak value is updated every mains cycle. When the 2-resistor system is used, the peak value is updated every half mains cycle, allowing a faster reaction to mains value changes.

The measured mains current level is used for the brownout/brownin detection and for the mains compensation in the PFC control loop.

Filter

The selected number of measurements value has a filtering effect.

A low value provides a faster response to changes. However, it also makes the system react to incidents (disturbances).

A high value shows a limited effect of incidents (or disturbances). However, it also leads to a slower reaction to changes.

16.3.4 Brownin level

Brownin

When the mains sensing current exceeds the selectable brownin level, the PFC can start operation.

Brownout

When the mains sensing current is below the selectable brownout level, the PFC stops operation. The behavior of the LLC converter at mains brownout can be set using the "disable LLC after mains brownout" function.

The brownout level selection is relative (and lower) to the brownin level. The brownin/brownout hysteresis provides the brownout level (see Section 8.3).

For example:

Brownin = 5.75 µA

Brownin/brownout hysteresis = 0.75 µA

Brownout = 5 µA

16.3.5 Brownout delay

When the mains voltage is below the brownout level for the selected amount of time, the system enters the brownout state.

The PFC converter stops operation. The behavior of the LLC converter at mains brownout can be set using the "disable LLC after mains brownout detection" function.

16.3.6 Brownin/brownout hysteresis

See Section 16.3.4.

16.3.7 Fast latch reset delay time

Reset a latch protection state

Two events can reset a latched protection:

- SUPIC drops to below the reset level
- Fast latch reset (FLR): a preset delay time after mains brownout detection

When the system is in latched protection, it is reset when the SUPIC voltage drops to the reset level. When the mains voltage is removed, the drop to the reset level occurs. However, discharging the SUPIC capacitor can take a long time.

To allow a fast reset of the latched protection, the mains sensing detects the disconnection of the mains voltage (brownout function). As soon as the disconnection of the mains voltage is detected, the latched protection is reset. When the mains is connected again, the reset allows a restart.

Fast latch reset delay time

A delay time can be selected using the fast latch reset delay time setting. When the mains voltage is below the brownout level and the system has stopped switching for this period, all protections are reset.

16.3.8 X-capacitor discharge delay time after AC off

When the SNSMAINS function detects that the mains is disconnected, the X-capacitor discharge is activated after a delay time that can be selected between 100 ms and 400 ms. Selecting infinite disables the X-capacitor discharge function.

16.4 PFC power factor improvement

The TEA2016AAT offers the possibility to increase/improve the power factor.

This function modifies the basic PFC operation to make the mains current more evenly divided like a sine wave over the mains voltage period. The method of modification is to increase the on-time of the PFC converter in the second half of each half (rectified) mains sine wave. The t_{on} increase can be selected to the best value for the corrections necessary for each application.

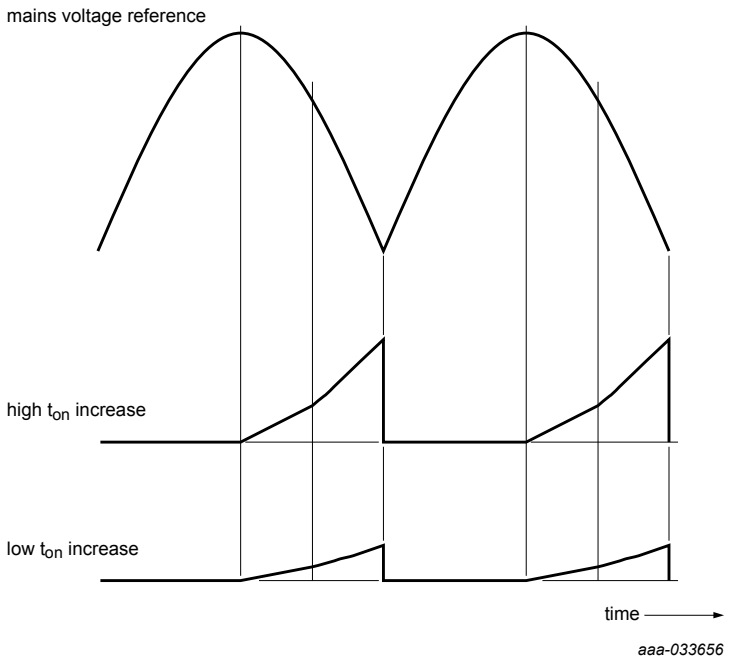


Figure 119. Power factor improvement by t_{on} increase

When this function is not required, selecting the option for "off" can disable it.

THD improvement

The t_{on} increase function can also be used to reduce the THD (harmonic distortion) of the mains, in combination with a higher value for the PFC maximum switching frequency limit setting.

16.5 PFC operation

16.5.1 PFC minimum off-time

To ensure that the TEA2016AAT operates in discontinuous or quasi-resonant mode, the PFC MOSFET is switched on after the transformer is demagnetized. The SNSCURPFC detects the PFC current I_{sense} with the voltage over a measurement resistor. When the voltage has increased to exceed −10 mV, demagnetization is detected on the SNSCURPFC pin.

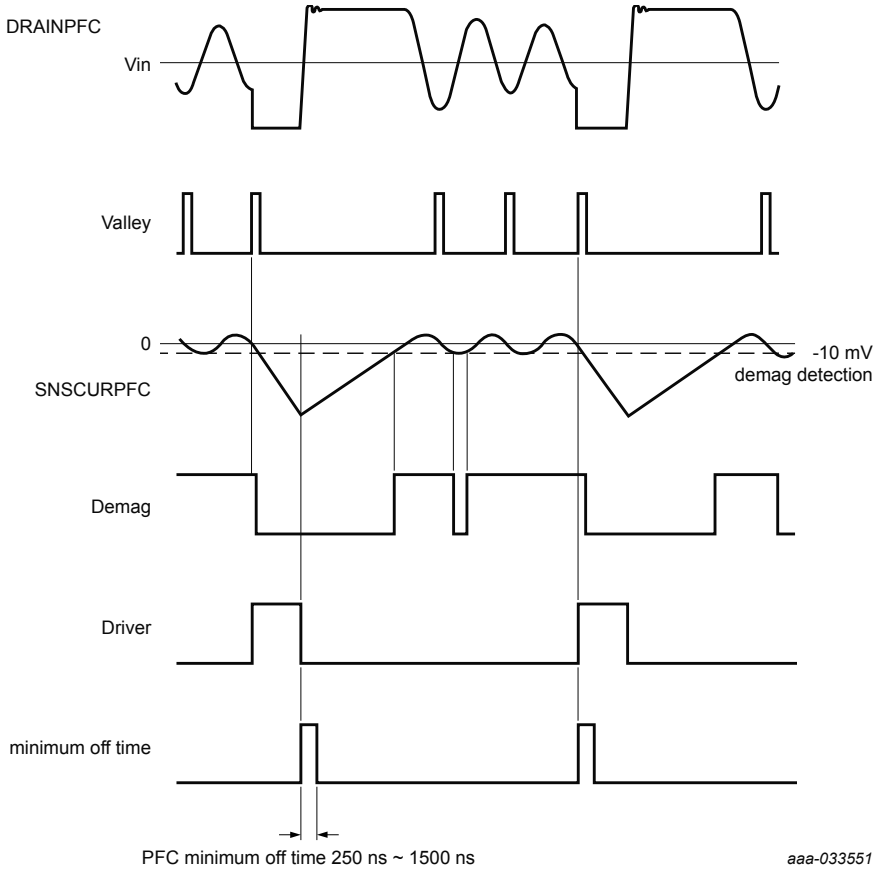


Figure 120. PFC control signals

Demagnetization timeout

When the PFC control does not detect demagnetization after the PFC MOSFET is switched off, a demagnetization signal is generated after a selectable maximum time (demagnetization timeout time). It prevents that the system stops if the signal is not detected because it has become too small.

PFC minimum off-time

After the PFC MOSFET is switched off, the MOSFET cannot be turned on again for a short time. This function prevents that the MOSFET can turn on immediately after switch-off because of false triggering of events (by disturbance signals). The time can be selected using the PFC minimum off-time setting.

16.5.2 Demagnetization timeout time

See Section 16.5.1.

16.5.3 PFC maximum switching frequency

To minimize PFC MOSFET switching losses, the switching frequency is limited to $f_{sw(PFC)max}$.

If the switching frequency for quasi-resonant operation exceeds the $f_{sw(PFC)max}$ limit, the system enters the discontinuous conduction mode (DCM). In general, the PFC MOSFET

switches on at a minimum voltage across the switch (valley switching). To limit the switching frequency when the maximum frequency value is reached, the system starts skipping valleys (switching on at the next valley).

The maximum switching frequency value can be selected.

Power factor, THD, and efficiency

The PFC maximum switching frequency and the t_{on} increase function can be used to reduce THD (harmonic distortion) and increase the power factor. A higher value for the PFC maximum switching frequency improves the power factor and THD. However, it reduces the efficiency at lower load conditions (and high mains voltages).

16.5.4 PFC ringing

To reduce switching losses and EMI, the PFC MOSFET switches on when the drain-source voltage is at its minimum (valley switching).

The valley detection is measured using the DRAINPFC pin. Two settings can be used to optimize the switching behavior to the converter properties related to ringing timing and amplitude.

16.5.4.1 Sensitivity valley detection

The sensitivity of the valley detection can be set using the parameter dV/dt ratio switch-on/maximum. This parameter can be used to optimize the switch-on in the valley in time.

If the valley is already detected before the minimum value is reached (too early), a higher value can compensate for it to obtain the best result.

16.5.4.2 PFC maximum ring time

If the amplitude of the ringing is too small to detect a valley, the controller generates an internal valley signal timeout after demagnetization is detected. This timeout value can be selected using the parameter PFC maximum ringing time (1/2). Normally, this function is only relevant in specific operating conditions where the ringing energy is very low.

16.5.5 PFC t_{on} max

The TEA2016AAT PFC operates under on-time control. The PFC MOSFET on-time is determined by:

- The digital error amplifier with a selectable general gain and a characteristic that depends on the SNSBOOST level.
- A linear relationship between the digital error amplifier output (PFCCOMP) and the intermediate on-time value. Selecting the maximum t_{on} value can modify the linear function. The result is a different gain for this section.
- Mains compensation using the SNSMAINS measurement.

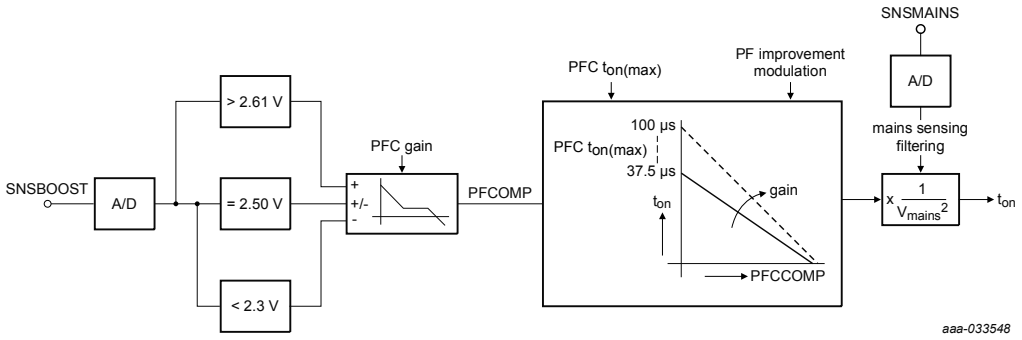


Figure 121. PFC t_{on} control

t_{on} max

When the on-time of the PFC MOSFET exceeds the maximum on-time, the PFC MOSFET is turned off and turned on again at the next cycle. The maximum on-time value can be set using a parameter. The result is a different gain.

16.5.6 PFC gain

See Section 16.5.5.

16.6 PFC protections

16.6.1 PFC OCP blacking time

To avoid false triggering of the PFC OCP function when turning on the PFC MOSFET, a short blanking time occurs after the PFC MOSFET is turned on. During this time, the internal OCP function cannot switch off the PFC MOSFET. The blanking time value can be selected using a parameter setting.

16.6.2 PFC OVP level

The PFC output voltage is measured via the SNSBOOST pin and the DRAINPFC pin. These independent functions provide a PFC output overvoltage protection (OVP) that is defined by a number of settings.

SNSBOOST: PFC OVP level

When an OVP is detected at the selected SNSBOOST pin voltage level, the PFC stops switching immediately. When the SNSBOOST voltage drops to below the regulation level (2.5 V), operation is continued again. For this function, there is no follow-up option for safe restart or latched.

One setting defines it:

- SNSBOOST PFC OVP level (2.6 V to 2.7 V)

OVP-DRAINPFC protection

For extra safety, a second independent overvoltage protection function is available on a different IC pin, DRAINPFC.

Four settings define it:

- OVP protection level
- Protection time delay
- Latched or safe restart
- Number of restarts before latched

It is a backup protection function for the OVP function on SNSBOOST. The DRAINPFC protection level is higher and selectable.

To avoid false triggering, a time delay can be set. When the time delay is set to infinite, the OVP-DRAINPFC function is disabled.

There is a follow-up option for safe restart or latched, including the possibility to allow a number of restarts before latched (see Figure 127).

16.7 PFC burst mode

16.7.1 PFC burst mode SNSBOOST ripple

When the LLC is in burst mode and the LLC burst duty cycle is below 50 %, the PFC enters burst mode. When the LLC is out of burst mode or the LLC burst duty cycle exceeds 75 %, it leaves burst mode.

Two types of PFC burst mode behavior

The PFC can operate in two types of burst mode. The type can be selected using the PFC burst mode SNSBOOST ripple setting.

Figure 122 shows the two types of PFC burst mode the behavior of the PFC in burst mode.

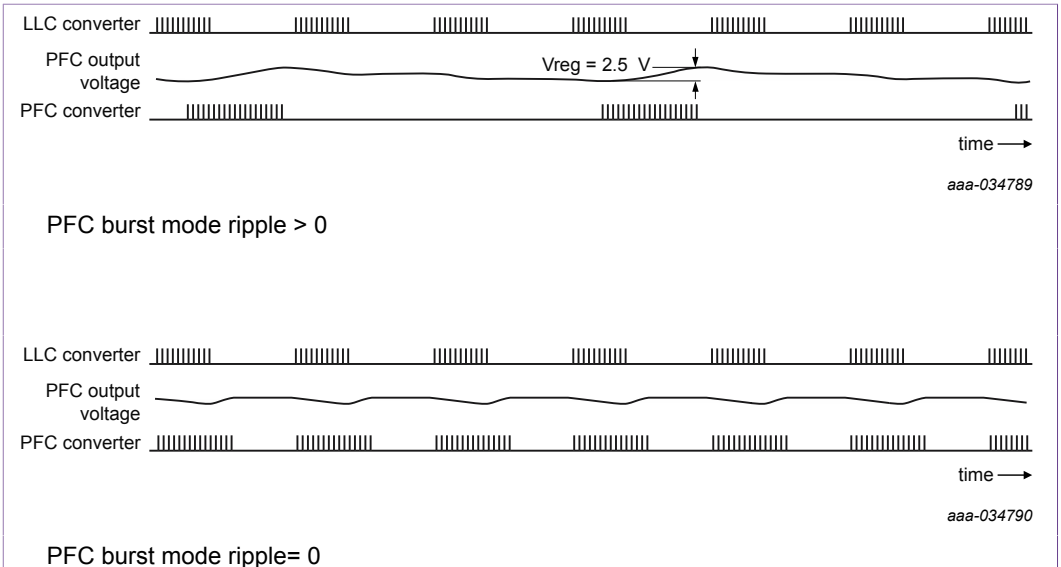


Figure 122. PFC burst mode by output voltage ripple or synchronous with LLC burst

PFC burst mode by output voltage ripple

The value for the PFC output voltage ripple can be set using the parameter PFC burst mode SNSBOOST ripple.

When the SNSBOOST voltage drops to below this level, the PFC starts switching. When it reaches the regulation level again, it stops switching.

A higher voltage ripple value reduces power consumption at (very) low load conditions. But it decreases PFC reaction time at load steps.

PFC burst mode synchronous with LLC burst

When the PFC burst mode SNSBOOST ripple value is set to zero, the PFC starts switching as soon as the LLC starts switching for a next burst. When the output voltage reaches the regulation level, the PFC stops switching.

The result of this type of PFC burst mode operation is less reduction of the power consumption compared to type with a high output voltage ripple value. But it provides a more stable and responsive converter operation.

PFC burst mode soft start and soft stop

To reduce the audible noise, a soft start and/or a soft stop can be added to the PFC burst. These functions can be activated using settings with a selectable value for the soft start/stop time.

The PFC on-time is increased (soft start) or reduced (soft stop) during the selected time. The selected time value is just an indicator during the resulting soft start/stop behavior, because the normal PFC regulation is active during this period and strongly influences the on-time.

16.7.2 PFC soft stop time burst mode

To reduce the audible noise, a soft start and/or a soft stop can be added to each PFC burst. Setting with a selectable value for the soft start/stop time can activate each function independently. The PFC on-time is increased (soft start) or reduced (soft stop) during the selected time. The selected time value is just an indicator during soft-start/ soft-stop behavior, because the normal PFC regulation is active during this period and strongly influences the on-time.

16.7.3 PFC soft-start time burst mode

To reduce the audible noise, a soft start and/or a soft stop can be added to each PFC burst. Settings with a selectable value for the soft start/soft stop time can activate each function independently. The PFC on-time is increased (soft start) or reduced (soft stop) during the selected time. The selected time value is just an indicator of the duration of the resulting soft start/stop behavior, because the normal PFC regulation is active during this period and strongly influences the on-time.

16.8 DRAINPFC OVP protection

16.8.1 PFC OVP-DRAINPFC (latched or safe-restart)

See Section 16.6.2.

16.8.2 OVP-DRAINPFC protection level

See Section 16.6.2.

16.8.3 OVP-DRAINPFC protection delay

See Section 16.6.2.

16.8.4 OVP-DRAINPFC number of restarts before latched

See Section 16.6.2.

16.9 LLC operation

16.9.1 Optocoupler current level

To achieve a low no-load input power, the current through the optocoupler must be set at a low level. However, depending on the selected optocoupler, a higher optocoupler current may be requested. The optocoupler current can be set at a level between 80 µA and 1200 µA (see Section 9.2.5).

16.10 LLC low-power mode

16.10.1 HP-LP transition level

The TEA2016AAT offers the possibility to make several independent choices for the transition levels of operation modes.

16.10.1.1 High-power mode

The HP-mode operates in continuous LLC switching with a 50 % duty cycle, which is similar to the traditional LLC operation via frequency control. The TEA2016AAT, however, obtains the result by VSNSCAP control driving for voltage levels on the resonant capacitor instead of switching by time/frequency.

In all operation modes, the VSNSCAP level determines when the gate drive is switched off. When the correct VSNSCAP level for the required output power is reached, the gate drive is switched off.

The adaptive non-overlap function based on the HB end-of-slope detection switches on the gate drive.

16.10.1.2 Low-power mode

The low-power mode is a burst mode at high repetition frequency. In this mode, to provide a better conversion efficiency, the energy in each pulse is kept relatively high.

During the not-switching period, the losses are low. The number of peaks that is skipped before starting a new LP cycle can set this period of not-switching.

16.10.1.3 HP-LP transition

The transition from HP-mode to LP-mode can be set at a certain power level using a parameter. To avoid unstable operation near the transition level, a hysteresis is applied.

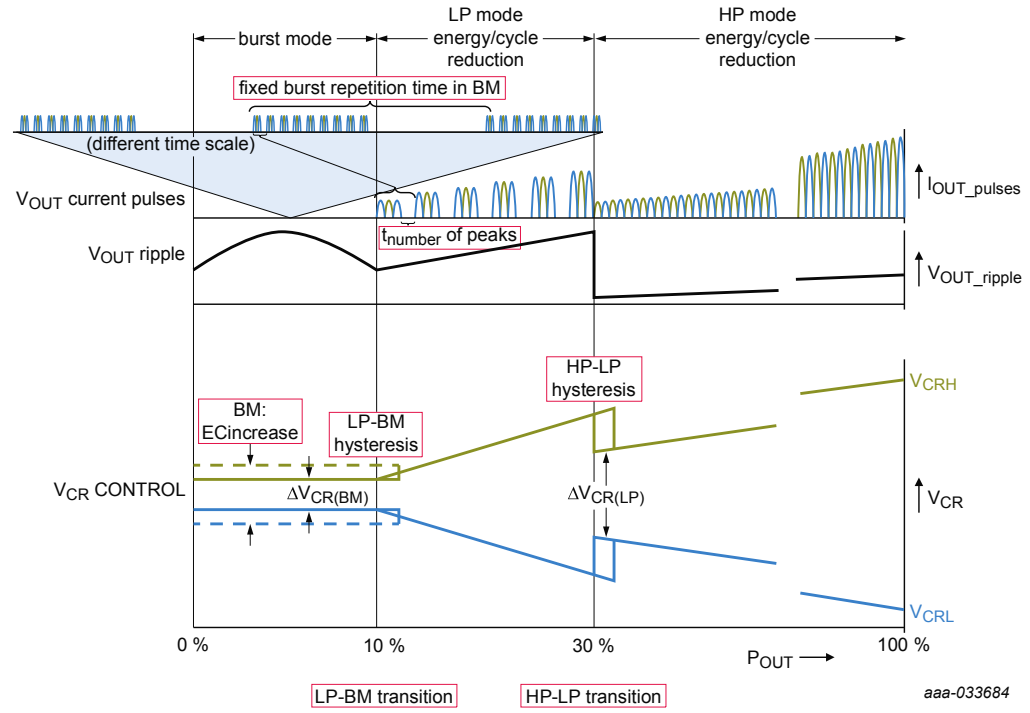


Figure 123. Operation modes and levels that can be modified using parameter settings

16.10.2 HP-LP hysteresis

The transition from HP-mode to LP-mode can be set at a certain power level using a parameter. To avoid unstable operation near the transition level, a hysteresis is applied. The amount of hysteresis can also be set using a parameter.

The value of the parameter is a percentage. It is the percentage that must be added to the HP-LP transition level to define the LP-HP transition level.

For example, if the HP-LP level is at 30 W and the hysteresis value is 20 %, the LP-HP transition is approximately 1.2 × 30 W = 36 W.

16.10.3 LP number of peaks

The low-power mode is a kind of burst mode at high repetition frequency. To provide a better conversion efficiency. In this mode, the energy in each pulse is kept relatively high.

During the non-switching period, the losses are low. The number of peaks that is skipped before starting a new LP cycle can set the period of non-switching.

Similar to BM operation, the LP mode increases the output voltage ripple. However, the resulting ripple increase is much lower than in BM. The number of peaks influence the LP output voltage ripple.

Because BM operation consists of series of LP cycles, the LP number of peaks setting slightly influences the total amount of output voltage ripple in BM operation.

A lower LP number of peaks value reduces the output voltage ripple.

16.10.3.1 A higher number of ringings

A higher number of ringings in combination with a high energy-per-cycle has a better efficiency at low loads. However, it also results in a lower repetition rate of the LP cycles. To avoid audible noise issues, the repetition frequency must not become lower than 20 kHz.

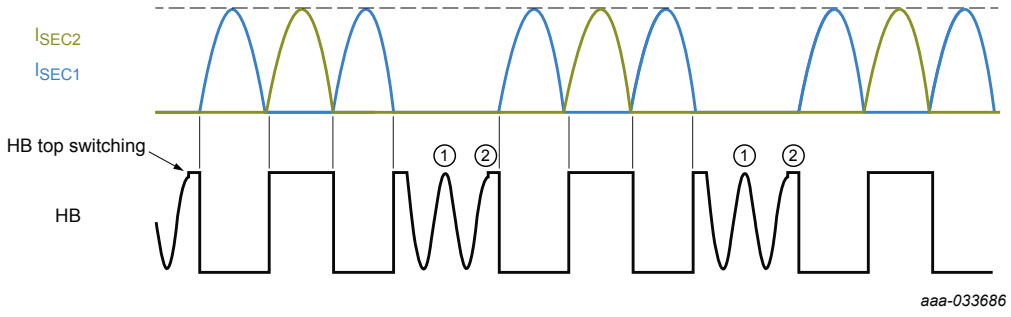
A higher number of ringings also leads to a higher output voltage ripple. A trade-off must be made for the balance of properties.

16.10.3.2 A low number of ringing

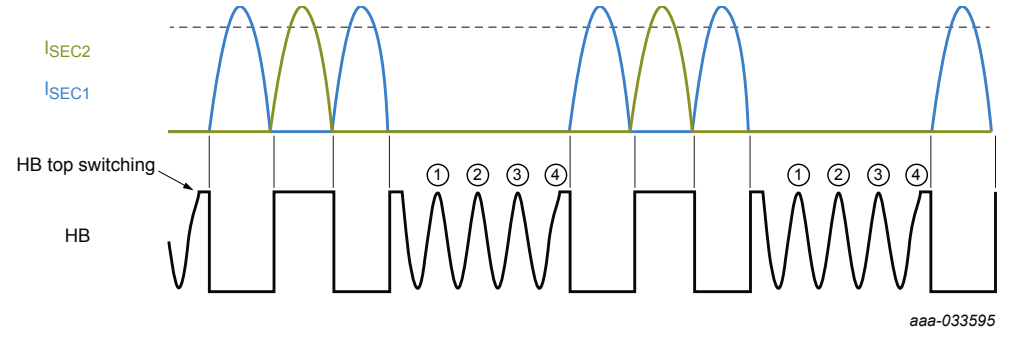
A low number of ringings results in a low output voltage ripple during LP mode operation. The gain in efficiency at low-power output can be less compared to a higher number of ringings. The amount also depends on the energy-per-cycle (energy to the output during each LP cycle).

16.10.3.3 Burst mode operation

BM operation consists of sequences of LP cycles. The LP switching defined by the number of peaks is also valid for the LP cycles in burst mode operation.



a. At the 2nd ringing peak



b. At the 4th ringing peak

Figure 124. LP mode operation starting a next cycle at the 2nd and the 4th HB ringing peak

16.10.4 V_{dump} level

To optimize the LP mode switching further in a specific application, the V_{dump} level can be used to find the best result for three equal output current pulses and no current to the output during the non-switching period. In most cases, optimizing for best efficiency is more important than obtaining the best looking switching sequence on the oscilloscope.

16.10.5 Zero-power slope

The TEA2016AAT also offers an option to disable burst mode operation with the LP-BM delay time option for infinite. For running stable at no load or very low load conditions in LP mode, the zero power slope setting of between 7 mV/s and 110 mV/s helps to optimize the operation for a specific application.

When this setting is modified for stable operation at no load or low load operation, the SNSCAP divider verification and dVcap offset optimization must be repeated.

When normal BM operation is used (keep the value at default), using this function is not necessary. Only when the time delay for BM is used, it is important to check if a different zero-power slope value is required.

16.11 LLC start-up

16.11.1 LLC soft start speed

The LLC soft-start speed defines the speed at which the converter lowers its switching frequency. A higher speed lowers the start-up duration. However, it can cause a high charge current and an overshoot at the output voltage. For the soft start, the speed can vary between 2x and 20x. In practice, it leads to an approximated start-up time of between 1 ms and 10 ms. However, the resulting start-up time depends on the converter behavior.

16.11.2 SNSBOOST compensation

A voltage ripple at the input of an LLC converter can result in a ripple in the output voltage. The TEA2016AAT measures the input voltage of the LLC via the SNSBOOST pin. To minimize the ripple at the output voltage, it has a feedforward compensation.

To prevent false protection triggering, the input voltage compensation also compensates for protection levels during (temporary) lower input voltages.

The level of compensation required depends on the external components. So it can be optimizes with a parameter that influences the amount of compensation (1.2 to 1.8).

Practical checking and optimizing

When running the LLC converter at a DC boost voltage, the most important mode transition levels and protection levels can be checked at different boost voltage levels. For example, nominal (400 V), nominal −10 % (360 V), and nominal −20 % (320 V). The transition/protection level for each test case can be optimized using the boost compensation function to become approximately the same.

16.11.3 Maximum (start-up) frequency

The maximum switching frequency of the LLC is limited to a value, which is defined with a parameter. This value also defines the maximum switching frequency during start-up. The maximum frequency can be set to between 150 kHz and 1000 kHz. Normally, settings above 500 kHz do not change the resulting behavior because of practical circuit limitations like time delays.

16.11.4 LLC current limit during start-up

At start-up, the LLC starts switching at the maximum frequency and ramps down the frequency until the ΔV_{SNSCAP} reaches the required level. If, during this start-up time, the primary current, which reflects the output current, reaches the selected maximum level, the power is temporarily not further increased (soft-start sweep is on hold) until the primary current drops to below this level again. This level is measured via the SNSCURLLC pin and can be selected to be between ±0.5 V and ±1.25 V on the 2.5 V bias level.

This level is different from the OCP level during operation (1.5 V; see Section 13.8.3).

16.12 LLC burst mode

16.12.1 LP-BM transition level

The basic preset of the LP-BM transition is done with a parameter between 1 % and 25 %. In the default BM configuration, the level of entering and leaving BM operation is the same. When the extra long waiting time in the last LP cycle has become zero when the output power is increased, the system has left BM operation and continues in LP mode by regulating the energy-per-cycle.

16.12.2 BM repetition frequency

In burst mode, each burst consists of a series of LP cycles. The burst is a period of LP switching. Each LP cycle in the burst contains the energy determined by the presetting of the minimum energy-per-cycle (EC_{MIN}) multiplied by a factor that can be selected (1× to 8×). The number of peak settings fixes the wait time of the LP cycle.

The BM fixed repetition frequency can be selected from 20 Hz to 3200 Hz.

To control the average output power, the number of LP cycles in a burst is now variable. An internal algorithm that targets the fixed repetition frequency for a burst determines the required number of LP cycles in the burst.

Extending the wait time of the last LP cycle obtains the non-switching period.

The value that can be selected for the minimum cycles in a burst ranges between 1 and 12. When this minimum value is reached and a further reduction of the power is necessary, extending the non-switching period reduces the repetition frequency. The BM repetition frequency has now become lower than the preset value.

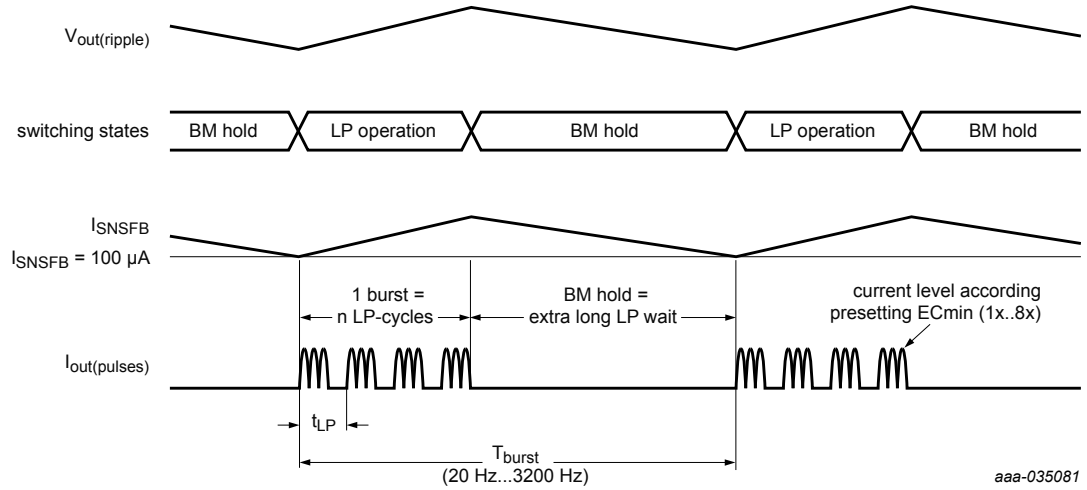


Figure 125. The burst mode system consists of LP switching and BM hold time

16.12.3 BM energy-per-cycle increase factor

See Section 16.12.2.

16.12.4 Minimum cycles in burst

See Section 16.12.2.

16.12.5 Burst on end optocurrent

When the system operates in burst mode, it adjusts the number of switching cycles such that burst frequency corresponds to the selected burst frequency. If, during these switching cycles, the output load decreases (load step), the output voltage increases as the system has calculated the number of required switching cycles. If the measured optocoupler current at the SNSFB pin exceeds a certain level, the system ends the burst switching cycle. This level can be between a factor of 2.5 and 7.5 times the selected optocoupler current level.

Higher BM repetition frequency

When a high output voltage ripple is allowed or when feedback regulation shows large overshoot/undershoot behavior, the feedback current can activate the burst on end function during each burst. The results is a higher BM repetition frequency than intended. To prevent a higher BM repetition frequency than intended, the factor can be increased.

16.12.6 Number of LLC BM soft-start cycles

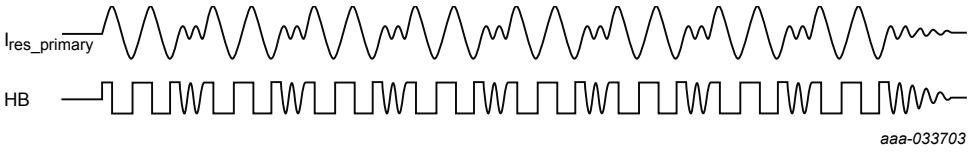
In burst mode operation, the converter is repetitively activated and stopped. The starting and stopping results in steep energy steps that can generate audible noise from the LLC transformer. The energy steps in the primary winding mainly have the risk of generating audible noise.

Soft start and soft stop

A soft start and a soft stop can effectively reduce the steep energy steps. These functions make the energy increase and decease gradually, therefore avoiding an energy step.

The TEA2016AAT offers settings to apply soft start and soft stop flexibility by defining the duration between 1 and 4 cycles. Figure 126 shows an example with four soft start cycles and two soft stop cycles.

Soft start and soft stop can be set independently. A soft start or soft stop can be applied independently or they can both be applied together. Selecting a value of 0 cycles can disable a soft start or soft stop.



a. Standard burst sequence

b. Burst sequence with soft start and soft stop

Figure 126. LLC burst mode setting examples for soft start and soft stop

Small effect on efficiency

Introducing a soft start and/or a soft stop causes a small reduction on the conversion efficiency. During soft start and soft stop, the primary current amplitude and the output current are reduced, which affects the efficiency during these cycles.

16.12.7 Number of LLC BM soft stop cycles

See Section 16.12.6.

16.12.8 LP-BM delay

To avoid that the system jumps between burst mode and low-power mode due to a small or a short transient at the output, which can cause audible noise, a delay can be set before the system enters burst mode. This time delay can be set between 0 s and 4 s. During this delay, the system keeps running in LP mode while reducing the energy-per-cycle to match the required output power down to zero.

16.12.9 BM-LP hysteresis and filter

BM-LP hysteresis

When the energy per cycle increase is set on a value higher than 1, the hysteresis function is active. When the system operates in burst mode and output power increases to exceed the LP-BM transition level plus a hysteresis level, the system enters the low-power mode. For the hysteresis level, a value of between 25 % and 100 % can be selected. It adds a percentage of the selected LP-BM transition percentage level.

Example:

If the rated output power at 100 % = 100 W, the LP-BM transition is set at 10 % and the hysteresis is set at 50 %. The system switches from burst mode to low-power mode at a 10 % + (50 % × 10 %) = 15 % which corresponds to 15 W output power.

For the resulting behavior from a practical measurement, see Section 13.4.5.

BM-LP hysteresis filter

To ensure a smooth transition when leaving burst mode and entering low-power mode, a burst-mode-to-low-power-mode transition filter can be set at between 2 and 8 cycles. When the output power exceeds the BM-LP transition level plus hysteresis for the selected number of burst cycles, it leaves the burst mode and enters the low-power mode.

16.13 LLC protections

16.13.1 LLC brownin SNSBOOST

To start LLC switching, the LLC brownin level defines the selectable minimum voltage (LLC brownin level) at the SNSBOOST pin. For this level, the following values can be selected: 2.1 V to 2.4 V.

16.13.2 LLC brownout SNSBOOST

When the voltage at the SNSBOOST drops to below a selectable level (LLC brownout: 1 V to 2.05 V), the LLC converter enters the protection state. When the SNSBOOST voltage exceeds the start level (LLC brownin) again, the LLC converter starts switching again.

16.13.3 SUPIC OVP level

In a resonant converter, the voltage at the SUPIC pin reflects the output voltage. When the SUPIC voltage exceeds a defined level, the OVP protection is triggered. The level can be set at 1 V to 15 V above the selected start level in steps of 1 V (see Section 10.5.3).

To avoid false triggering, a delay can be set from 10 µs to 800 µs. The response of this protection can be latched, safe restart, or latched after several restart trials. Setting the delay to infinite can disable this OVP function (see Section 10.5.3).

16.13.4 SUPIC OVP (latched or safe-restart)

As follow-up of this protection a safe restart or a latched protection can be selected. For the latched protection choice, the option to make a number of safe restarts before the latched protection becomes active is available.

16.13.5 SUPIC OVP number of restarts to latch

If a latched protection is set, a number of safe restarts (1 to 16) can be done before the latched protection becomes active. If the latched protection must become active immediately, the value can be set to 0.

When no protection was triggered during a period of 5 seconds after a restart, the counter value for the number of restarts is reset to zero.

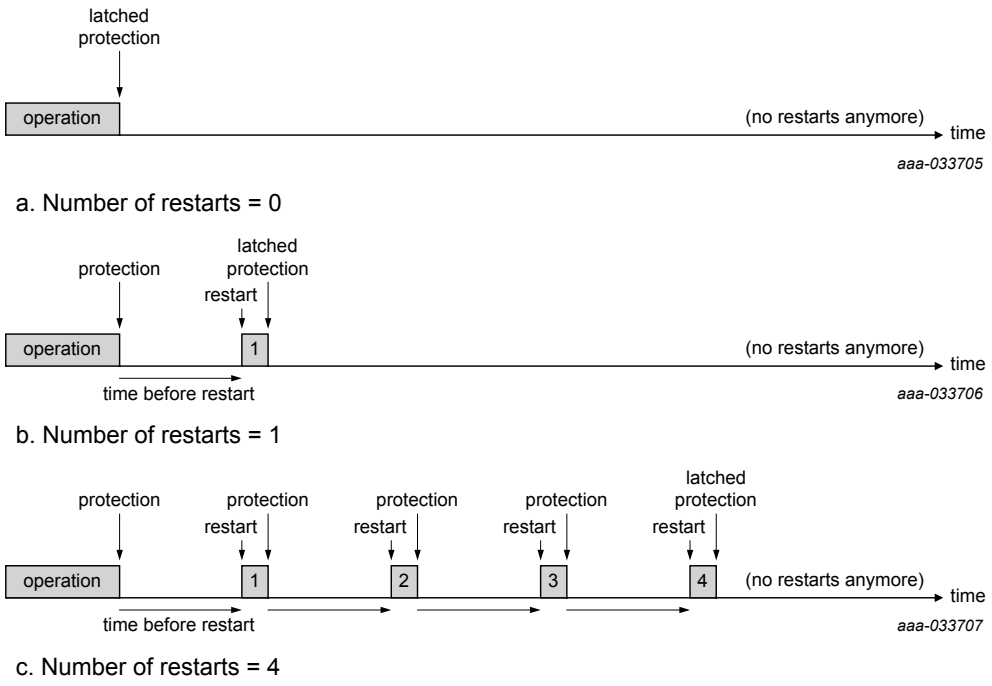


Figure 127. Number of restarts before latched

16.13.6 LLC OCP filter

The primary LLC current is sensed on SNSCURLLC. If the measured voltage on R_m exceeds the overcurrent level of ±1.5 V (4 V or 1 V on SNSCURLLC), the corresponding switch (GATELS/GATEHS) is turned off. However, the system continuous switching. In this way, the primary current is limited to the OCP level. If the OCP level is exceeded for a selectable number (5 to 1000) of consecutive cycles (GATELS and/or GATEHS), the system stops switching and enters the protection mode (see Section 10.5.8).

Setting the filter value on infinite disables the LLC OCP function for protection. The current limiting function remains.

16.13.7 OCP LLC latched or safe restart

As follow-up of this protection a safe restart or a latched protection can be selected. For the latched protection choice, the option to make a number of safe restarts before the latched protection becomes active is available.

16.13.8 LLC OCP number of restarts to latch

As follow-up of this protection, a safe restart or a latched protection can be selected. For the latched protection choice, the option to make a number of safe restarts before the latched protection becomes active is available (see Figure 127).

16.13.9 Capacitive mode regulation level

The primary current is measured accurately, cycle-by-cycle, for the internal switching logic. Two comparators with a selectable level between 20 mV and 160 mV above and below the bias voltage of 2.5 V detect when the primary current is nearing capacitive mode operation. When this level is reached before the VCAP control switch off the gate,

the capacitive mode prevention forces a switch-off to prevent capacitive mode switching (see Section 9.9).

16.13.10 Power limitation level

The controller limits the maximum output power of the converter. The limitation ensures that the applied load is below the maximum rating of selected components. The V_{cap} control does not drive the power to above the preset SNSCAP levels. When the output current is above this power limit, the result is that the output voltage drops accordingly. The limit for the maximum output power can be selected between 100 % and 200 %.

The OPP functions are defined with this maximum power level as a reference.

The power limit function can be used for engineering purpose to verify, so it matches the internal levels.

16.13.11 Start OPP 1 timer

The TEA2016AAT offers the possibility to define two independent overpower protection (OPP) functions. Most systems require only one OPP function. In this case, the "OPP time 2 to protect" value can be set to infinite.

The definition of the OPP function consists of two setting values:

- The power level at which the protection timer is activated (Start OPP timer level): 0 % to 50 %.
- Time until the protection is activated and the system stops operation (OPP time to protect): 50 ms to 3000 ms.

The OPP power level is defined relative to the power limit setting.

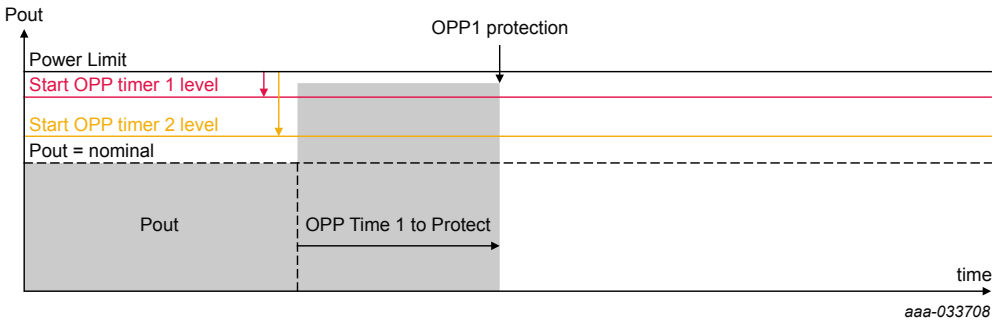
Example:

If the power limit setting is 170 % and the Start OPP timer 1 level is set to −20 %, OPP timer 1 starts at 170 % − (0.2 × 170) % = 136 %.

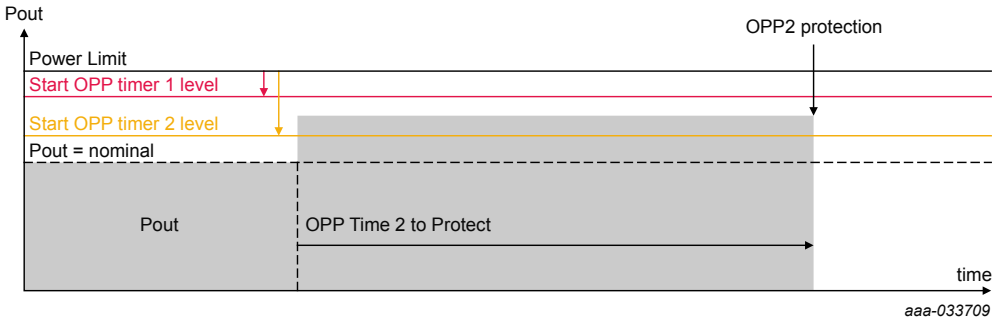
2 OPP functions: OPP1 and OPP2

In a system with two OPP functions, OPP1 is usually chosen at a higher power level with a shorter time to protection. OPP2 is chosen at a lower power level allowing a longer time to protection.

Both OPP functions are independent and can be set according to the system requirements.



a. OPP1 protection



b. OPP2 protection

Figure 128. OPP1 and OPP2: example of a typical choice for 2 different protection levels and 2 different times to protection

Selecting an infinite time to protect disables the OPP functions.

16.13.12 OPP 1 time to protect

See Section 16.13.13.

16.13.13 Start OPP 2 timer

See Section 16.13.13.

16.13.14 OPP 2 time to protect

See Section 16.13.13.

16.13.15 OPP latched or safe-restart

As follow-up of this protection a safe restart or a latched protection can be selected. For the latched protection choice, the option to make a number of safe restarts before the latched protection becomes active is available.

16.13.16 OPP number of restarts to latch

If a latched protection is set, a number of safe restarts (1 to 16) can be made before the latched protection becomes active. If the latched protection must become active immediately, the value can be set to 0 (see Figure 127).

16.13.17 HB minimum non-overlap time

To ensure that the GATEHS is properly turned off before the GATELS is turned on, and vice versa, there is a selectable minimum non-overlap time of between 50 ns and 200 ns.

16.13.18 HB maximum non-overlap time

When the system does not detect an end of slope at the HB node after turning off the GATEHS pin, the system turns on the GATELS after the maximum non-overlap time and vice versa. The selectable value for this timeout is between 500 ns to 1100 ns.

16.13.19 LLC maximum on-time

When the on-time of the GATELS or GATEHS exceeds the maximum on-time, the switch is turned off and the LLC converter starts the next cycle. This timeout setting can be between 10 µs and 40 µs.

16.13.20 Disable LLC after mains brownout

When the mains is disconnected, the PFC stops switching after its brownout delay. Normally, the LLC converter continues switching until the input voltage of the LLC drops to below a minimum level. Especially for a minimum load at the output, the LLC dropping to the minimum level can take a long time.

When a brownout is detected at the mains input, a timer can be initialized that also disables the LLC converter. For this time, values between 125 ms and 6000 ms can be selected. The option that the LLC converter remains switching until its input voltage drops to below a minimum level can be set by selecting off.

16.13.21 Disable LLC after SNSBOOST OVP

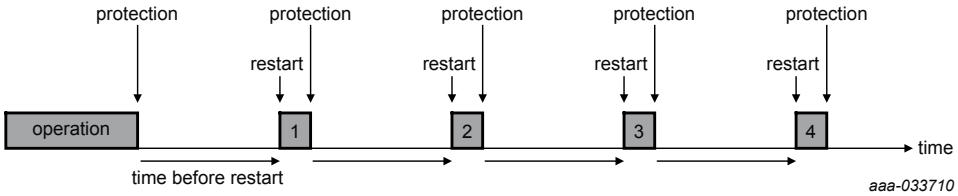
When an OVP is detected on the SNSBOOST pin, the PFC always stops switching. The response of the LLC can be set to either continue operation or to stop switching until the voltage on the SNSBOOST pin drops to the PFC output voltage regulation level.

A delay time can be set between 5 ms and 1250 ms. Or the function can be disabled by selecting off.

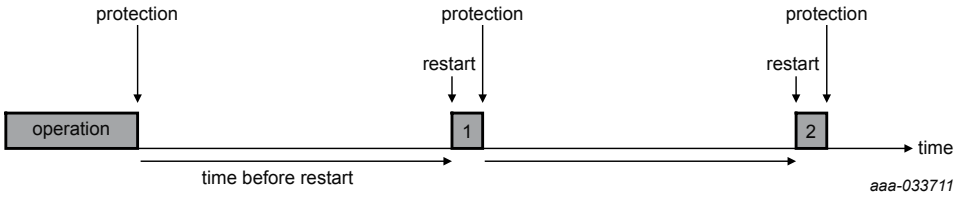
16.14 General protection settings

16.14.1 Safe restart timer

When the system is in protection mode and the triggered protection is preset for safe restart as a follow-up, it restarts after a selectable safe-restart time between 0.5 s and 10 s.



a. Short safe-restart timer value



b. Long safe-restart timer value

Figure 129. Safe restart timer behavior

16.14.2 Down counts per up count

When the number of triggers is being counted to a certain preset value for protection, changes in triggering in time can occur. Sometimes the protection level is triggered and sometimes not. For the down-count-per-up-count setting, a selection between 1 and 8 can be made to filter the events.

For example, if the value is 2, it means for each event that does not exceed the protection levels, two events must exceed the level to reach the same counter value again.

16.14.3 Fast disable function on SNSBOOST

By pulling down SNSBOOST, the system operation can be stopped. How this function behaves can be determined with the options below:

- On/off:
  When SNSBOOST becomes low, immediate stop. When SNSBOOST is released, a start-up occurs again.
- Safe restart:
  When SNSBOOST becomes low, immediate stop. Follow-up with safe restart until SNSBOOST is released.
- Latched:
  When SNSBOOST becomes low, immediate stop. Follow-up with a latched protection.

16.15 External OTP

16.15.1 External OTP current level

The external application temperature is measured via an NTC connected to the SNSMAINS pin. To measure the external NTC value, an internal current is used. The value of this current that can be selected is between 150 µA and 1050 µA.

Selecting 0 µA disables the external OTP function.

16.15.2 External OTP delay time

To avoid false triggering of the external OTP, a delay time of between 0.5 s and 8 s can be set. Because the NTC measurement follows the mains cycles, the OTP delay time can deviate slightly because of the mains frequency.

16.15.3 OTP latched or safe restart

The follow-up of this protection can be selected to be safe restart or a latched protection. For the latched protection choice, the option to make a number of safe restarts before the latched protection becomes active is available (see Figure 127).

16.15.4 OTP number of restarts to latch

If a latched protection is set, a number of safe restarts (1 to 16) can be made before the latched protection becomes active. If the latched protection must become active immediately, the value can be set to 0.

When no protection was triggered during a period of 5 seconds after a restart, the counter value for the number of restarts is reset to zero.

16.16 Power good

For housekeeping of the total system, a power good signal can be used to communicate a basic message to the application that is supplied by the power supply.

- Power delivery is stable after start-up; power supply is OK
- Power delivery goes down (soon); power supply is (soon) not OK

The TEA2016AAT supports such a function by making the SNSFB output pin voltage high or low, depending on the state of the power supply. The SNSFB pin is also used for LLC feedback regulation by the SNSFB current.

The SNSFB output is made active high after start-up. This condition shows that the converter output voltage is not yet OK because the system is in a start-up condition. The default delay time is 5 ms (see Figure 131)

After start-up, when the system enters the operating state, the SNSFB output is pulled low to show that the SNSFB voltage output is OK.

The combined power good and SNSFB functions are shown in Figure 130.

A pull-up circuit on primary and secondary side, connected by an optocoupler, provides the power good signal to the application that is supplied by the power supply.

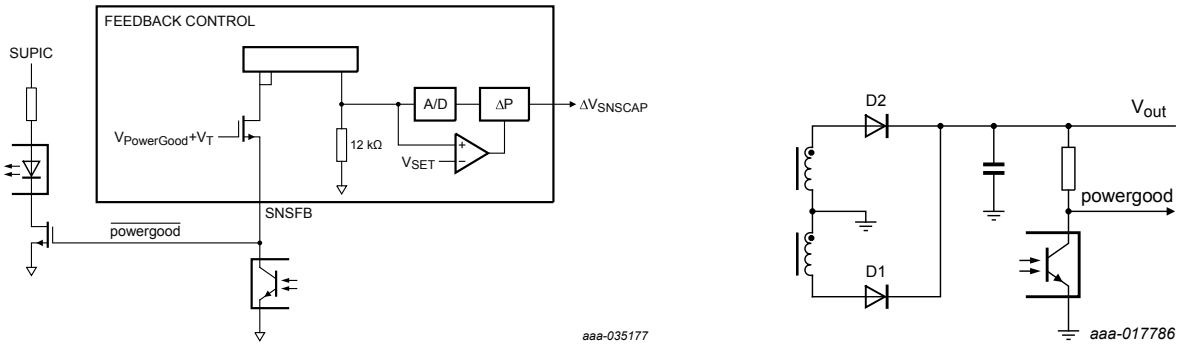


Figure 130. Power good combined on SNSFB

Figure 6 shows the combination of SNSFB current for regulation and the voltage for power good in a timing sequence during start-up, protection, and stop operation.

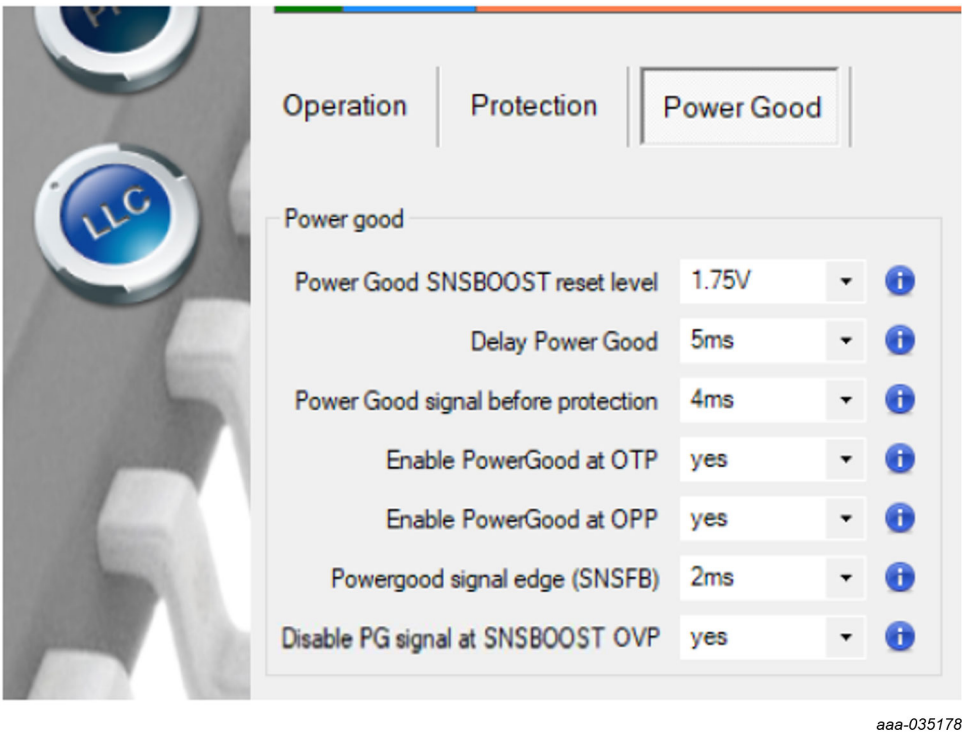


Figure 131. Power good settings

In alignment with the selected option for several parameters, the SNSFB voltage becomes active high when:

- The voltage on the SNSBOOST pin drops to below 1.75 V (default value)
- The OPP counter is close to its end value (default is yes; default is 4 ms in advance)
- The converter is about to stop due to an OTP protection (default is yes; default is 4 ms in advance)
- When the system enters the protection mode (OVP, OCP, or UVP), it pulls high the SNSFB pin and stops switching immediately.

To avoid any disturbance of the regulation loop (SNSFB current), the increase and decrease of the SNSFB voltage is in alignment with a predefined ramp (default setting

is 2 ms). The options for different values are intended to optimize the transition of the resulting power good signal on the secondary side.

The best choice of settings for the power good parameters mainly depends on system requirements from the application that is powered by the power supply.

16.16.1 Delay power good

When the output voltage is in regulation after start-up, power good indicates that the output voltage is in regulation. A delay can be set between the time the output voltage reaches the regulation level and the transition of the power good signal. This delay can be set between 0 ms and 1000 ms.

16.16.2 Power good SNSBOOST reset level

When the measured voltage at the SNSBOOST pin drops to below the selected LLC brownout level, the LLC converter stops switching. Normally, it occurs because of a disconnected mains.

When the converter is switched off due to this LLC brownout detection, the power good signal can give a prewarning. When the voltage at the SNSBOOST pin drops to below a selectable value (SNSBOOST = 1.1 V to 1.9 V), the power good feature is triggered.

16.16.3 Power good signal before protection

The power good signal gives a prewarning when the converter is switched off due to an OPP, OTP, or UVP SNSBOOST protection. This signal is activated at a time that can be set between 2 ms and 8 ms.

16.16.4 Enable PG at OTP

When the converter is switched off because of an OTP detection, the power good signal can give a prewarning. The OTP can be an internal or an external OTP.

The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good signal before protection setting (Section 16.16.3). This function can be enabled or disabled.

16.16.5 Enable PG at OPP

When the converter is switched off due to an OPP detection, the power good signal can give a prewarning. The prewarning can be given when the output power exceeds the OPP level1 or OPP level2 for the defined time.

The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good signal before protection setting. This function can be enabled or disabled.

16.16.6 Disable PG at SNSBOOST OVP

The TEA2016AAT offers a setting to stop LLC operation at an SNSBOOST OVP (see Section 16.13.21). Using this setting can cause the output voltage to drop. Together with the setting for LLC, the PG can be set to provide a PG signal at this event or not.

16.16.7 Power good signal edge on SNSFB

The power good function and the feedback network are connected at the SNSFB pin.

To avoid that a trigger of the power good function disturbs the regulation loop (SNSFB current), the time for its transition must be relatively long. The predefined and selectable value is between 1 ms and 4 ms.

17 Application example: TEA2016DB1519v2 240 W power supply

17.1 Circuit diagrams

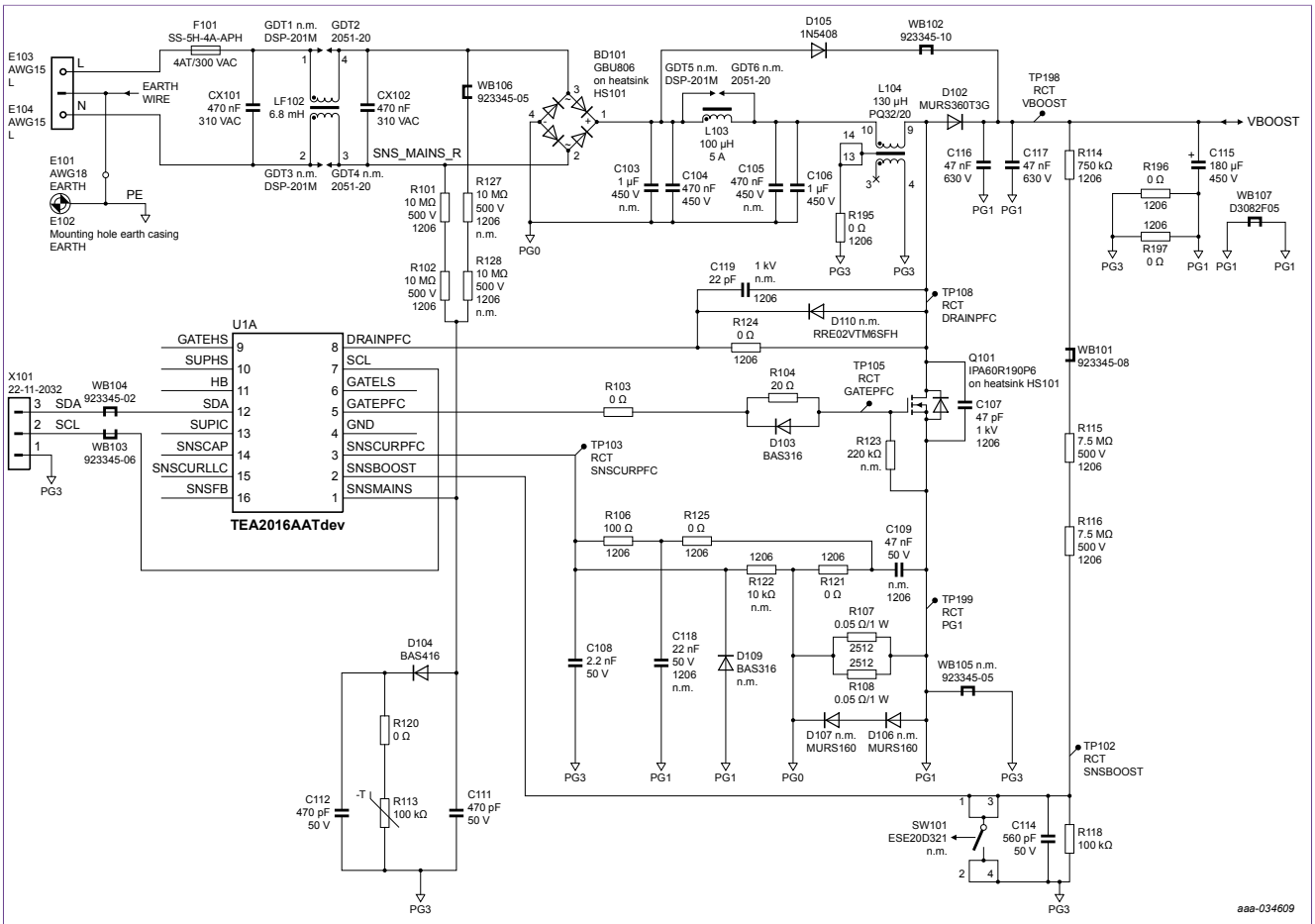


Figure 132. TEA2016DB1519v2, 240 W power supply (PFC part)

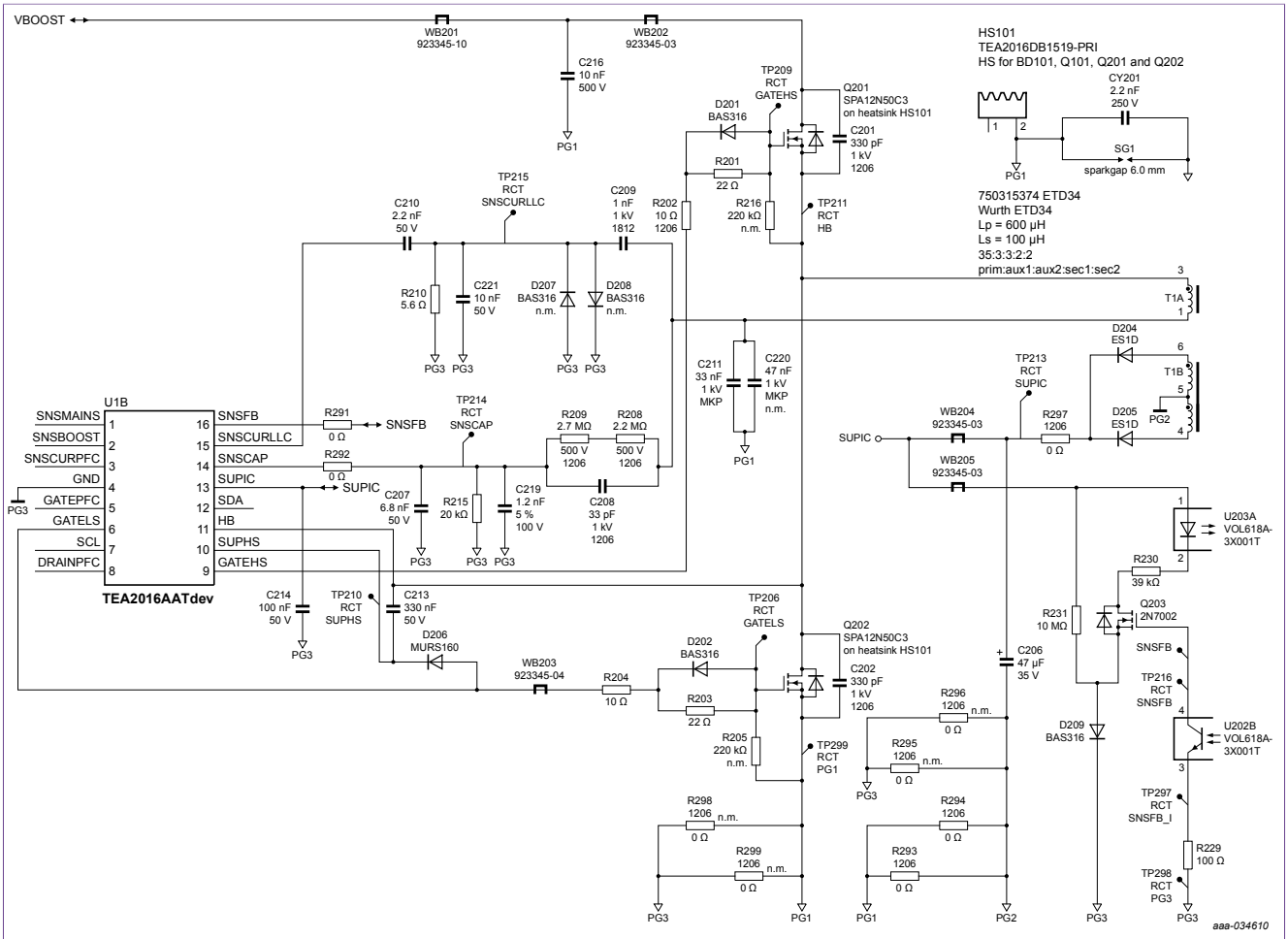


Figure 133. TEA2016DB1519v2 240 W power supply (LLC part)

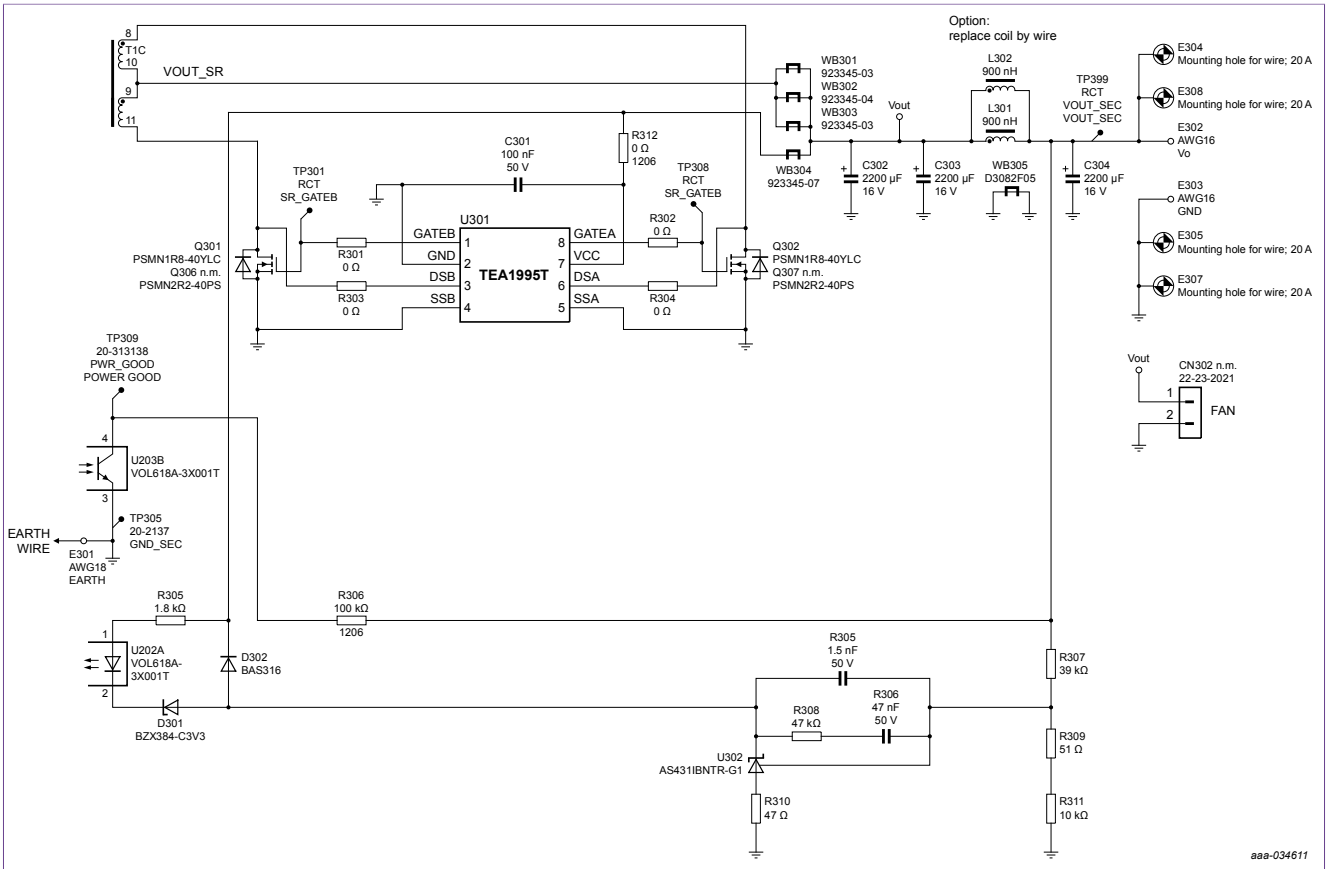


Figure 134. TEA2016DB1519v2 and TEA2016AAT 240 W power supply (SR part)

17.2 Circuit diagrams with function descriptions

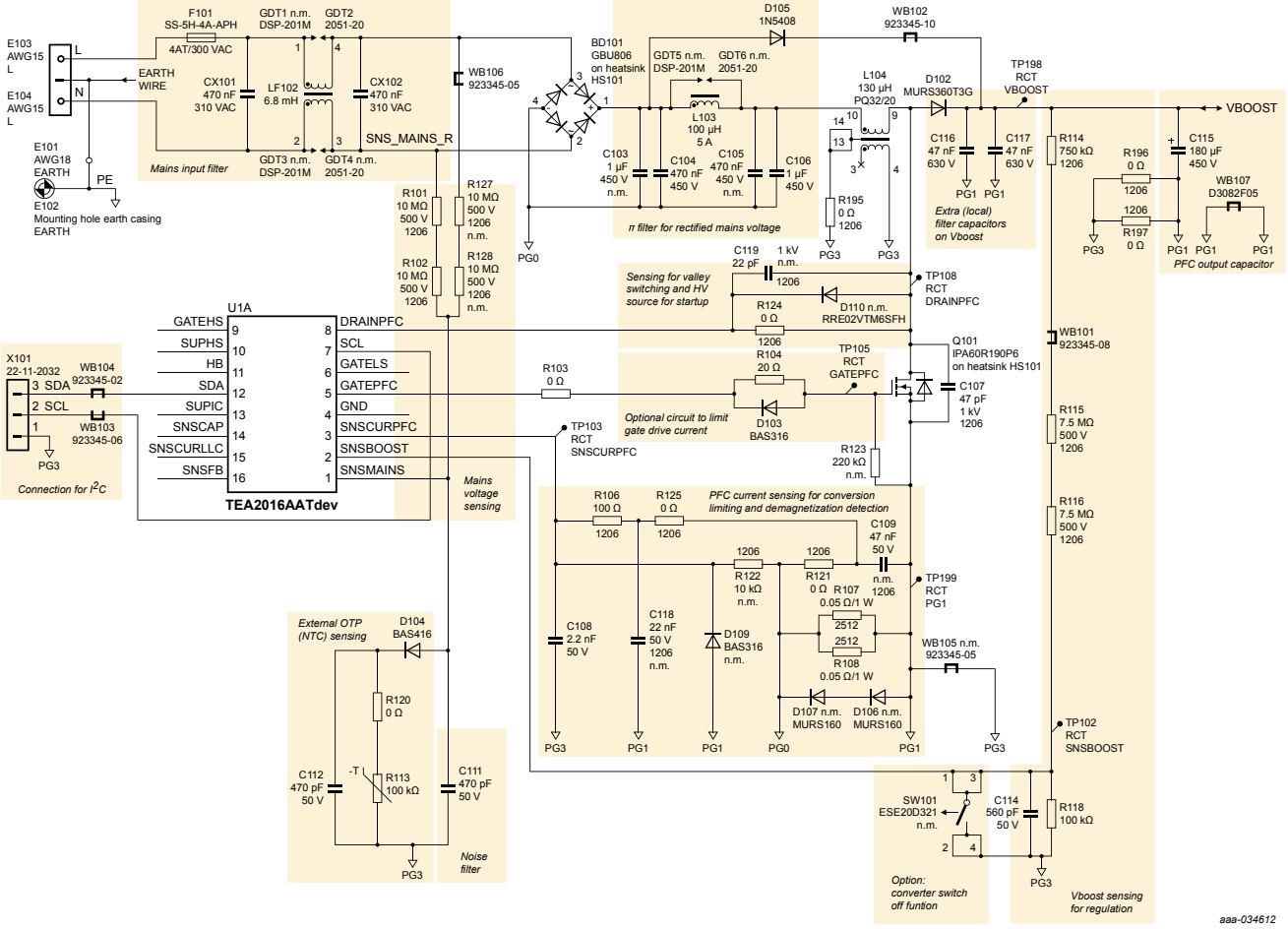


Figure 135. TEA2016DB1519v2 240 W demo board (PFC part)

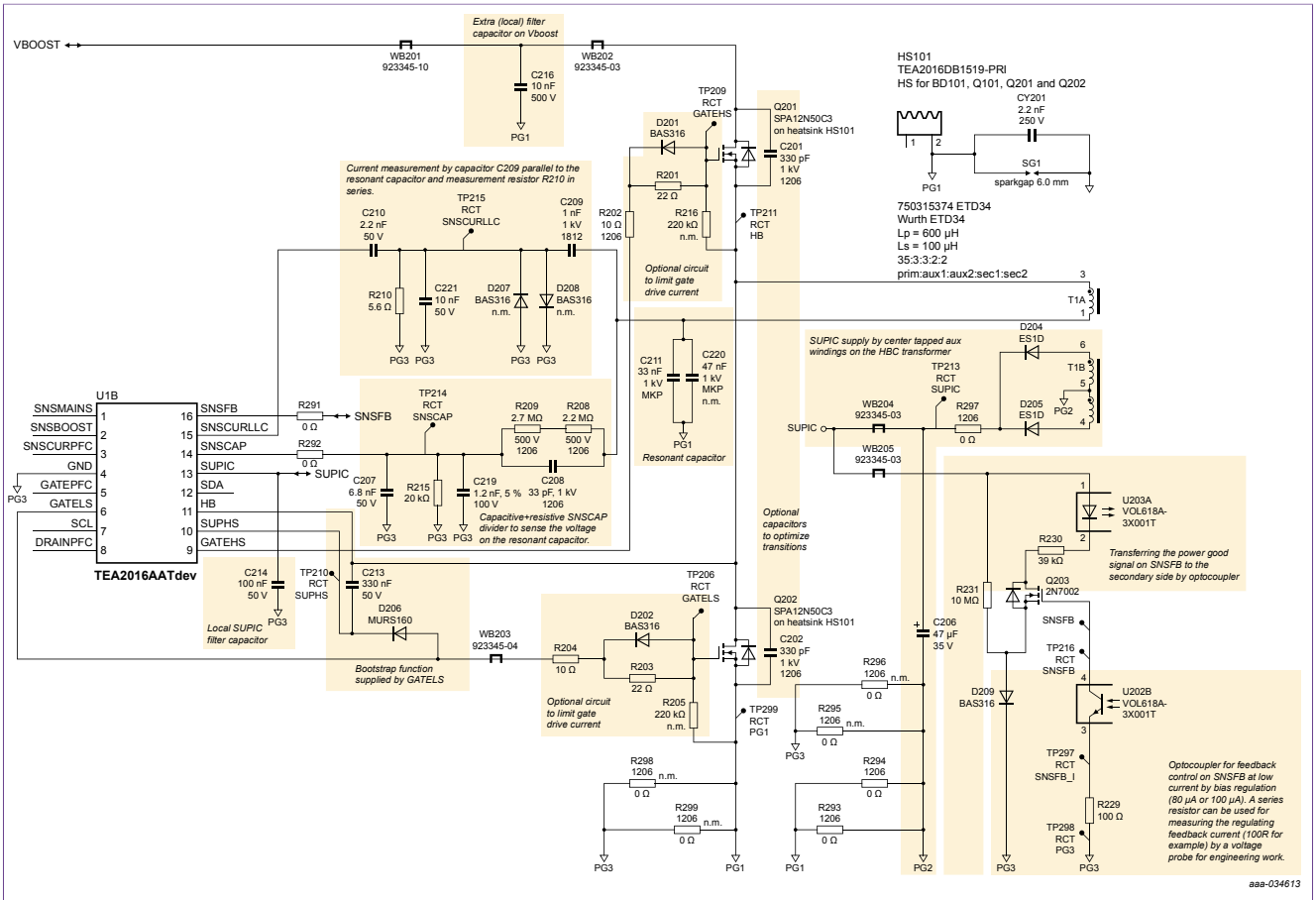


Figure 136. TEA2016DB1519v2 240 W demo board (LLC part)

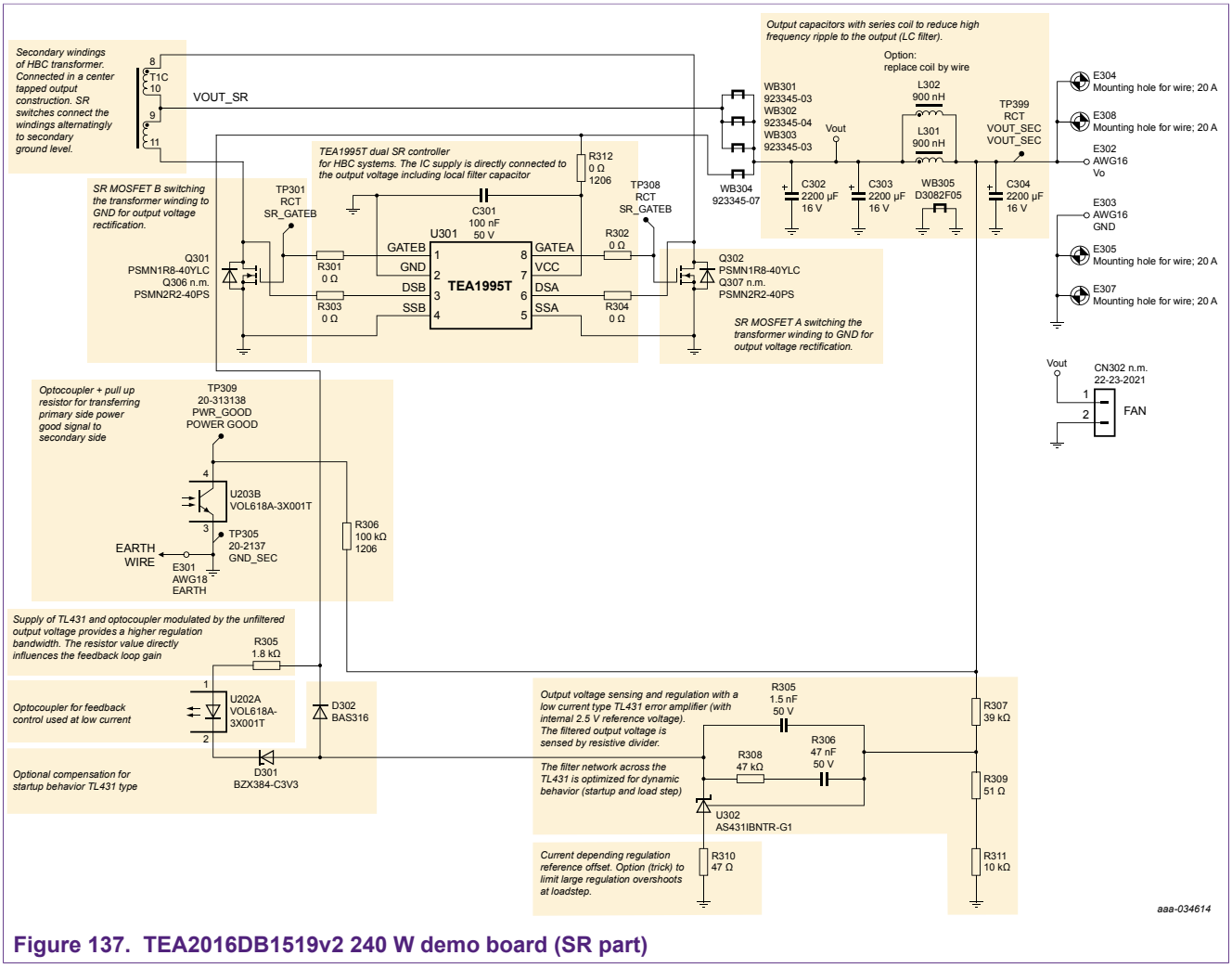
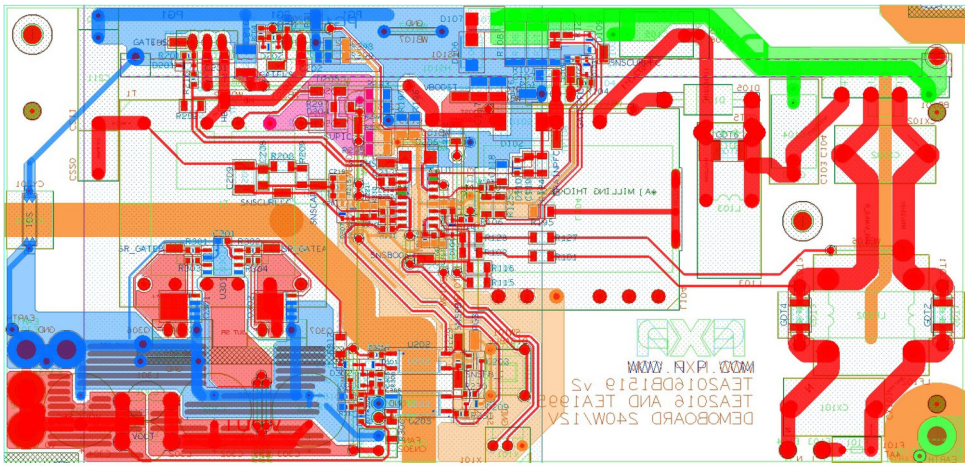


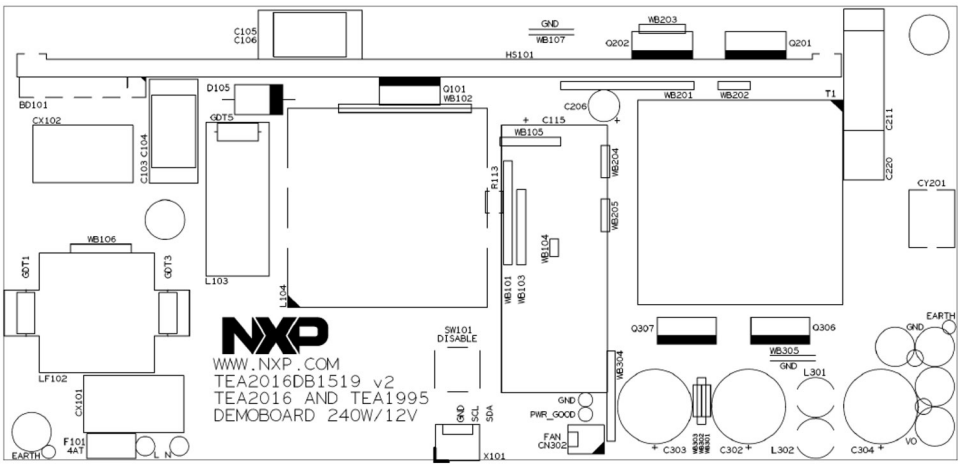
Figure 137. TEA2016DB1519v2 240 W demo board (SR part)

17.3 PCB layout TEA2016DB1519v2 240 W demo board



aaa-034615

a. PCB layout



aaa-034616

b. PCB components

Figure 138. TEA2016DB1519v2 PCB layout and components

18 TEA2016AAT MTP parameter settings

Table 12 shows a list of the parameters in the MTP. It shows the Ringo GUI parameter name, the NXP Semiconductors parameter name, and the value.

The Ringo GUI export function can generate a list with the MTP settings of an IC. It provides an overview of the selected values and can be used for comparison, checking or sharing the information. In addition to this list, the settings can be stored as a .mif file. This file can be reloaded in the Ringo GUI software later or shared with others.

Table 12. Ringo parameter/IC parameter settings

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
1	PFC OCP	pfc_ocp	OK	-	0
2	PFC OVP (drainPFC)	pfc_ovp_suphv	OK	-	0
3	PFC OVP (SNSBOOST)	pfc_ovp_snsboost	OK	-	0
4	LLC OPP 1	llc_opp1	OK	-	0
5	LLC OPP 2	llc-opp2	OK	-	0
6	LLC maximum start-up time	llc_max_startup_time	OK	-	0
7	LLC OCP	llc_ocp	OK	-	0
8	LLC OVP	llc_ovp_prot	OK	-	0
9	external OTP	ext_otp	OK	-	0
10	internal OTP	int_otp	OK	-	0
11	fast disable	fast_disable	OK	-	0
12	LLC maximum on-time	llc_max_on_time	OK	-	0
13	LLC maximum I_{opto}	llc_max_iopto	OK	-	0
14	LLC capacitor mode	llc_cap_mode	OK	-	0
15	MTP read failure	mtp_read_fail	OK	-	0
16	OPP via SUPIC UVP	opp_via_supic_uvp	OK	-	0
17	read lock	read_lock	reading is enabled	-	0
18	write lock	write-lock	writing is enabled	-	0
19	SUPIC start level	sup_start	19	V	0
20	low SUPIC during energy save	dis_vlow	enabled	-	0
21	X-capacitor discharge delay-time after AC-off	t_xcap_disch	200	ms	0
22	mains resistor value	rmains	20	MΩ	0
23	PFC maximum switching frequency	max_pfc_freq	125	kHz	2
24	PFC burst mode SNSBOOST ripple	vburst_ripple	70	mV	0
25	PFC soft-stop time burst mode	t_burst_stop	normal	-	0
26	dV/dt ratio switch-on/maximum	ratio_valley_detect	0.5	-	0
27	mains SNS filtering	mains_filter	2	-	0

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
28	PFC gain	pfc_gain	0.75	-	0
29	power factor improvement	pf_compensation	off	-	0
30	mains SNS resistors	nr_mains_resistors	1 resistor	-	0
31	PFC soft-start time burst mode	t_burst_start	normal	-	0
32	maximum (start-up) frequency	max_llc_startup	350	kHz	0
33	LLC soft-start speed	llc_tsoftstart	7x	-	0
34	LLC soft-start current limit	max_llc_istartup	0.75	V	0
35	V_{dump} level	vdump	2.6	V	0
36	minimum non-overlap time	t_no_min	200	ns	0
37	maximum non-overlap time	t_no_max	1.1	µs	0
38	maximum on-time	llc_max_on	20	µs	0
39	capacitive mode regulation level	capm_lvl	100	mV	0
40	optocoupler current level	iopto	80	µA	0
41	HP-LP transition level	hp_lp_lev	30	%	0
42	LP-BM transition level	lp_bm_lev	10	%	0
43	HP-LP hysteresis	hp_lp_hys	20	%	0
44	dV_{cap} offset	vcap_offset	0	mV	0
45	zero power slope	min_slope	6	mV/µs	0
46	LP-BM delay time	lp_bm_del	0	s	0
47	BM-LP hysteresis	bm_lp_hys	50	%	0
48	BM-LP hysteresis filter	bm_lp_filt	4	-	0
49	BM frequency	bm_freq	800	Hz	0
50	BM energy-per-cycle increase	bm_incr	1	-	0
51	number of soft-start cycles	start_cycle_sel	0	-	0
52	number of soft-stop cycles	stop_cycle_sel	0	-	0
53	safe restart timer 1	sr_time__r1_	1	s	0
54	safe restart timer 2	sr_time__r2_	1	s	0
55	safe restart timer 3	sr_time__r3_	1	s	0
56	safe restart timer 4	sr_time__r4_	1	s	0
57	slope of the 4th BM soft-stop cycle	stop_cycle4	180	-	0
58	slope of the 3rd BM soft-stop cycle	stop_cycle3	1	-	1
59	slope of the 2nd BM soft-stop cycle	stop_cycle2	84	-	0
60	slope of the 1st BM soft-stop cycle	stop_cycle1	36	-	0
61	slope of the 4th BM soft-start cycle	start_cycle4	36	-	0
62	slope of the 3rd BM soft-start cycle	start_cycle3	84	-	0
63	slope of the 2nd BM soft-start cycle	start_cycle2	1	-	1

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
64	slope of the 1st BM soft-start cycle	start_cycle1	180	-	0
65	number of BM soft-stop cycles	nr_bm_sstop	2	-	2
66	number of BM soft-start cycles	nr_bm_sstart	2	-	2
67	minimum cycles in burst	min_nr_cycl	3	-	0
68	burst-on end by optocurrent	iopto_bm_end	2.5	-	0
69	LP number of peaks	lp_nr_peaks	2	-	0
70	SNSBOOST compensation	snsb_comp	−1.4	-	0
71	fast latch reset delay time	t_flr	50	ms	0
72	external OTP current level	eotp_lvl	600	µA	0
73	external OTP delay time	t_eotp	4	s	0
74	OTP	otp_ltch__r1_	safe restart	-	0
75	OTP	otp_ltch__r2_	latched	-	1
76	OTP	otp_ltch__r3_	latched	-	1
77	OTP	otp_ltch__r4_	latched	-	1
78	OTP number of restarts to latch	otp_nr_rest	0	-	0
79	brownin level	brownin_lvl	5.7	µA	0
80	brownin/brownout hysteresis	brownin_hys	0.75	µA	0
81	brownout delay	t_brownout	50	ms	0
82	PFC OCP blanking time	ocp_tblank	300	ns	0
83	PFC maximum on-time	ton_max	50	µs	0
84	PFC OVP level	ovp_lvl	2.63	V	0
85	OVP-drainPFC protection level	ovpprot_lvl	475	V	0
86	OVP-drainPFC protection delay	t_ovpprot	infinite	ms	3
87	PFC OVP-drainPFC	ovp_ltch__r1_	safe restart	-	0
88	PFC OVP-drainPFC	ovp_ltch__r2_	safe restart	-	0
89	PFC OVP-drainPFC	ovp_ltch__r3_	safe restart	-	0
90	PFC OVP-drainPFC	ovp_ltch__r4_	safe restart	-	0
91	OVP-drainPFC number of restarts before latched	ovp_nr_rest	0	-	0
92	PFC maximum ringing time (½)	max_tring_pfc	10	µs	0
93	PFC minimum off-time	tmin_off	1500	ns	0
94	maximum start-up time	t_start_max	100	ms	0
95	LLC maximum ringing time	max_tring_llc	5	µs	0
96	LLC brownout level (SNSBOOST)	snsb_stop	1.65	-	3
97	LLC brownin level (SNSBOOST)	snsb_start	2.3	V	2
98	disable LLC after mains brownout	llc_dis_bo	250	ms	0
99	disable LLC after SNSBOOST OVP	dis_ovp_snsb	off	-	3

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
100	power limitation level	pow_lim	155	%	0
101	start OPP timer 1	opp1_lvl	−20	%	0
102	OPP time 1 to protect	opp1_time__r1_	50	ms	0
103	OPP time 1 to protect	opp1_time__r2_	50	ms	0
104	OPP time 1 to protect	opp1_time__r3_	100	ms	2
105	OPP time 1 to protect	opp1_time__r4_	50	ms	0
106	count down value at 1 cycle below OPP	opp_nr_dwn	1	-	0
107	start OPP timer 2	opp2_lvl	−10	%	0
108	OPP time 2 to protect	opp2_time	infinite	-	0
109	OPP	opp_ltch__r1_	safe restart	-	0
110	OPP	opp_ltch__r2_	safe restart	-	0
111	OPP	opp_ltch__r3_	safe restart	-	0
112	OPP	opp_ltch__r4_	latched	-	1
113	OPP restarts to latch	opp_nr_rest	0	-	0
114	OVP level	llc_ovp	10	V	0
115	OVP delay	llc_tovp	50	µs	0
116	down counts per up count OVP	llc_ovp_nr_dwn	1	-	0
117	OVP	llc_ovp_ltch__r1_	safe restart	-	0
118	OVP	llc_ovp_ltch__r2_	latched	-	1
119	OVP	llc_ovp_ltch__r3_	latched	-	1
120	OVP	llc_ovp_ltch__r4_	latched	-	1
121	OVP restarts to latch	llc_ovp_nr_rest	0	-	0
122	LLC OCP	llc_ocp_ltch__r1_	safe restart	-	0
123	LLC OCP	llc_ocp_ltch__r2_	safe restart	-	0
124	LLC OCP	llc_ocp_ltch__r3_	safe restart	-	0
125	LLC OCP	llc_ocp_ltch__r4_	latched	-	1
126	OCP restarts to latch	llc_ocp_nr_rest	0	-	0
127	fast disable by SNSBOOST	llc_fast_disable	latched	-	3
128	power good signal before protection	pgd_tim	4	ms	0
129	enable power good at OTP	pgd_otp	yes	-	0
130	enable power good at OPP	pgd_opp	yes	-	0
131	power good SNSBOOST reset level	pgd_lvl	1.75	V	0
132	delay power good	pgd_del	5	ms	0
133	power good signal edge (SNSFB)	pgd_tr	2	ms	0
134	disable power good signal at SNSBOOST OVP	pgd_ovp_sbo	yes	-	0

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
135	PFC operation	pfc_dis_dev	enabled	-	0
136	overcurrent protection filter LLC	llc_tocp__r1_	5	-	0
137	overcurrent protection filter LLC	llc_tocp__r2_	5	-	0
138	overcurrent protection filter LLC	llc_tocp__r3_	5	-	0
139	overcurrent protection filter LLC	llc_tocp__r4_	5	-	0
140	vendor code	mtp_code	0x0001	-	1

19 MTP bitmap

The bitmap in Figure 139 shows the location of each parameter in the MTP memory.

Page		Bit number															
(dec)	(hex)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31	1F	MTP code															
30	1E					llc_tocp(R4)			llc_tocp(R3)			llc_tocp(R2)			llc_tocp(R1)		
29	1D	pfc_dis_dev	Pgd_OVP_SBO	Pgd_tr		Pgd_del			Pgd_lvl					Pgd_OPP	Pgd_OTP	Pgd_tim	
28	1C						llc_fast_disable		llc_ocp_nr_rest		llc_ocp_ltch_(R4)	llc_ocp_ltch_(R3)	llc_ocp_ltch_(R2)	llc_ocp_ltch_(R1)			
27	1B		llc_ovp_nr_rest		llc_ovp_ltch_(R4)	llc_ovp_ltch_(R3)	llc_ovp_ltch_(R2)	llc_ovp_ltch_(R1)	llc_ovp_nr_dwn		llc_tovp			llc_ovp			
26	1A					opp_nr_rest		opp_ltch (R4)	opp_ltch (R3)	opp_ltch (R2)	opp_ltch (R1)	opp2_time			opp2_lvl		
25	19			opp_nr_dwn		opp1_time (R4)			opp1_time (R3)			opp1_time (R2)			opp1_time (R1)		
24	18										opp1_lvl				pow_lim		
23	17	dis_ovp_snsb			LLC_dis_bo		snsb_start		snsb_stop			max_tring_llc		t_start_max		tmin_off	
22	16	max_tring_pfc				OVP_nr_rest		OVP_ltch (R4)	OVP_ltch (R3)	OVP_ltch (R2)	OVP_ltch (R1)	t_OVPprot		OVPprot_lvl		OVP_lvl	
21	15	ton_max		ocp_tblank				t_brownout			brownin_hys			brownin_lvl			
20	14					otp_nr_rest		otp_ltch (R4)	otp_ltch (R3)	otp_ltch (R2)	otp_ltch (R1)	t_eotp			eotp_lvl		
19	13											t_flr			snsb_comp		
18	12			lp_nr_peaks			lopto_bm_end		min_nr_cycl			nr_bm_sstart			nr_bm_sstop		
17	11	stop_cycle1				start_cycle2				start_cycle3				start_cycle4			
16	10									stop_cycle1				stop_cycle2			
15	0F	start_cycle3				stop_cycle4											
14	0E					sr_time (R4)			sr_time (R3)			sr_time (R2)			sr_time (R1)		
13	0D	stop_cycle_sel			start_cycle_sel			bm_incr			bm_freq					bm_lp_filt	
12	0C	bm_lp_hys		lp_bm_del			min_slope					vcap_offset				hp_lp_hys	
11	0B									lp_bm_lev				hp_lp_lev			
10	0A					lopto			capm_lvl			llc_max_on		t_no_max		t_no_min	
9	9						Vdump			max_llc_lstartup		llc_tsoftstart			max_llc_freq		
8	8	t_burst_start		Nr_mains resistors		PF compensation			PFC_gain		Mains_filter			Ratio_valley_detect			
7	7	t_burst_stop		Vburst_ripple		max_pfc_freq		Rmains	t_xcap_disch				dis_vlow	sup_start	write_lock	read_lock	
6	6	opp_via_supic_uvp	mtp_read_fail	llc_cap_mode	llc_max_iopto	llc_max_on_time	fast_disable	int_otp	ext_otp	llc_ovp_prot	llc_ocp	llc_max_startup_time	llc_opp2	llc_opp1	pfc_ovp_snsboost	pfc_ovp_suphv	pfc_ocp

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Figure 139. MTP bitmap customer section

20 Abbreviations

Table 13. Abbreviations

Acronym	Description
ADT	adaptive dead time
ASIC	application-specific integrated circuit
BM	burst mode
CMR	capacitive mode regulation
ECmin	minimum energy-per-cycle
HBC	half-bridge converter
HP	high-power mode
HV	high voltage
IC	integrated circuit
LCD	liquid crystal display
LLC	resonant tank or converter (L_m+L_r+C_r in series)
LP	low power
MHR	mains harmonics reduction
MTP	multiple times programmable
NTC	negative temperature coefficient (resistor)
OCP	overcurrent protection
OLP	open-loop protection
OPP	overpower protection
OPTO	optocoupler
OTP	overtemperature protection
OVP	overvoltage protection
PCB	printed-circuit board
PG	power good
PFC	power factor correction
QR	quasi-resonant mode
SCP	short-circuit protection
SMD	surface-mounted device
SR	synchronous rectification
UVP	undervoltage protection

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Date of release: 28 November 2019
Document identifier: AN12330